

In-DRAM Signature Generation Using Simultaneous Multiple-Row Activation

An Experimental Study of Off-The-Shelf DRAM Chips

Umut Başer

İsmail Emir Yüksel F. Nisa Bostancı Konstantinos Sgouras

Ataberk Olgun Emre H. Demirli Zhiheng Yue Harsh Songara

Oğuz Ergin Onur Mutlu

SAFARI

ETH zürich

 **kasirga**



TOBB ETÜ
University of Economics & Technology

Outline

Motivation

DRAM Organization & Operation

SiMRA-PUF

Testing Methodology

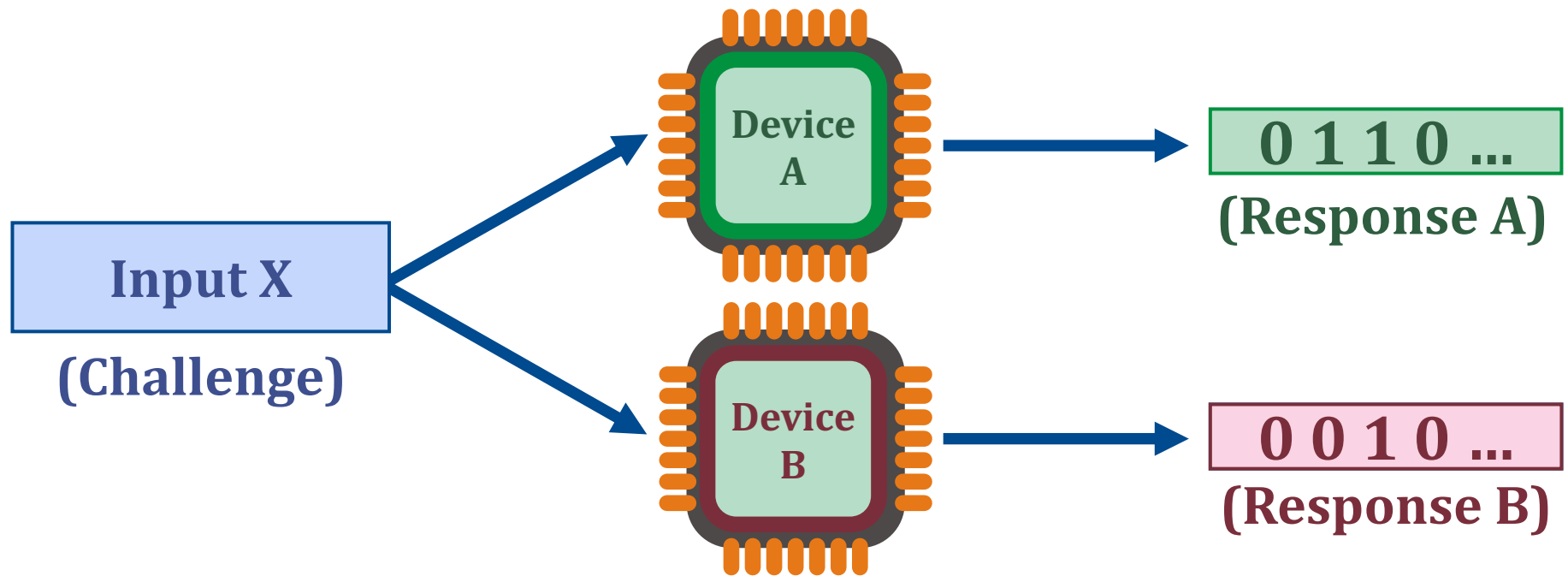
Real DRAM Chip Results

Conclusion

Physical Unclonable Functions (PUFs)

A PUF uses **unique physical variations** of the device to generate **unique signatures (responses)**

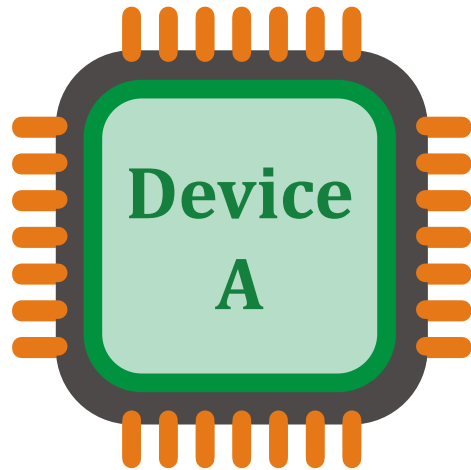
- **Same device**, same challenge → **same response**
- **Any other device**, same challenge → **different response**



Physical Unclonable Functions (PUFs)

These properties make PUFs suitable for many applications:

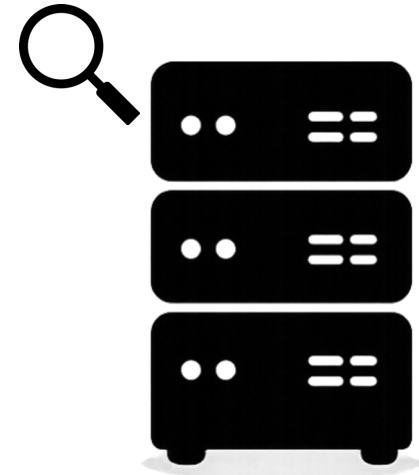
- **Device Authentication**



Challenge_x

Output:
PUF Response_x

Device A	Response X
Device A	Response Y
...	...
Device B	Response X



Trusted Device

Physical Unclonable Functions (PUFs)

These properties make PUFs suitable for many applications:

- **Device Authentication**
- **Cryptographic Key Generation**
- **Intellectual Property Protection**
- **Hardware Obfuscation**
- ...

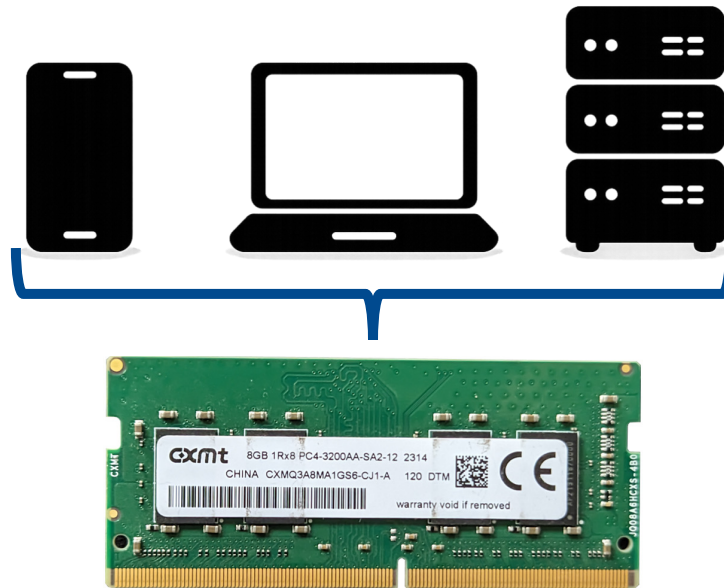
Due to these applications,
many different PUFs have been proposed
by both industry and academia

DRAM-Based PUFs

DRAM-based PUFs enable generating PUF responses within **DRAM chips**

DRAM is **ubiquitous** in modern computing platforms

Low Cost: No specialized hardware needed for PUFs



DRAM-Based PUFs

Prior work exploits different sources of manufacturing variations to develop DRAM-based PUFs by:

- Using start-up values
- Disabling DRAM refresh
- Violating timing parameters
- Storing and sensing fractional voltage levels
- ...

We propose using a recently discovered phenomenon called **Simultaneous Multiple-Row Activation (SiMRA)** to generate **device-specific signatures**

Outline

Motivation

DRAM Organization & Operation

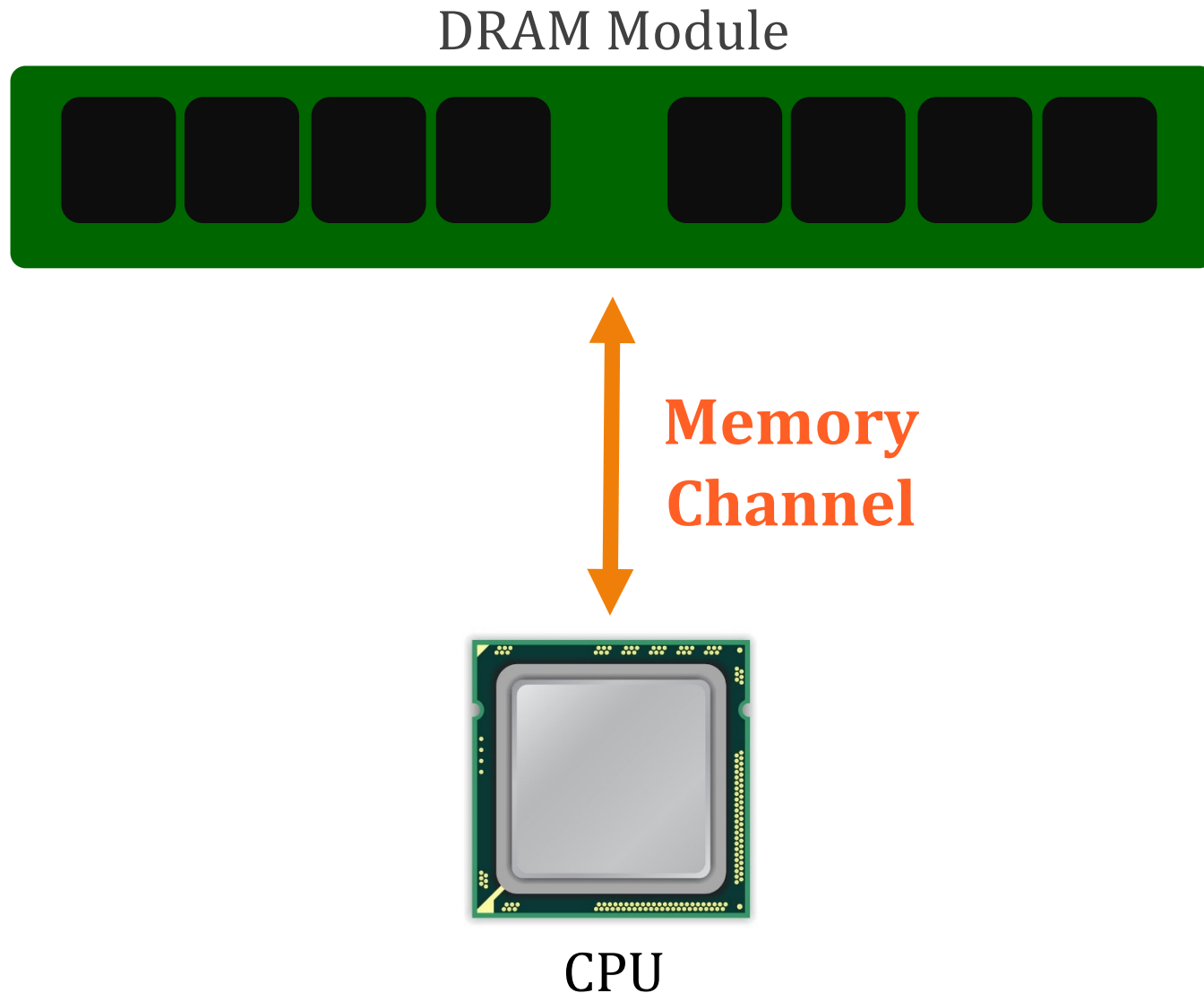
SiMRA-PUF

Testing Methodology

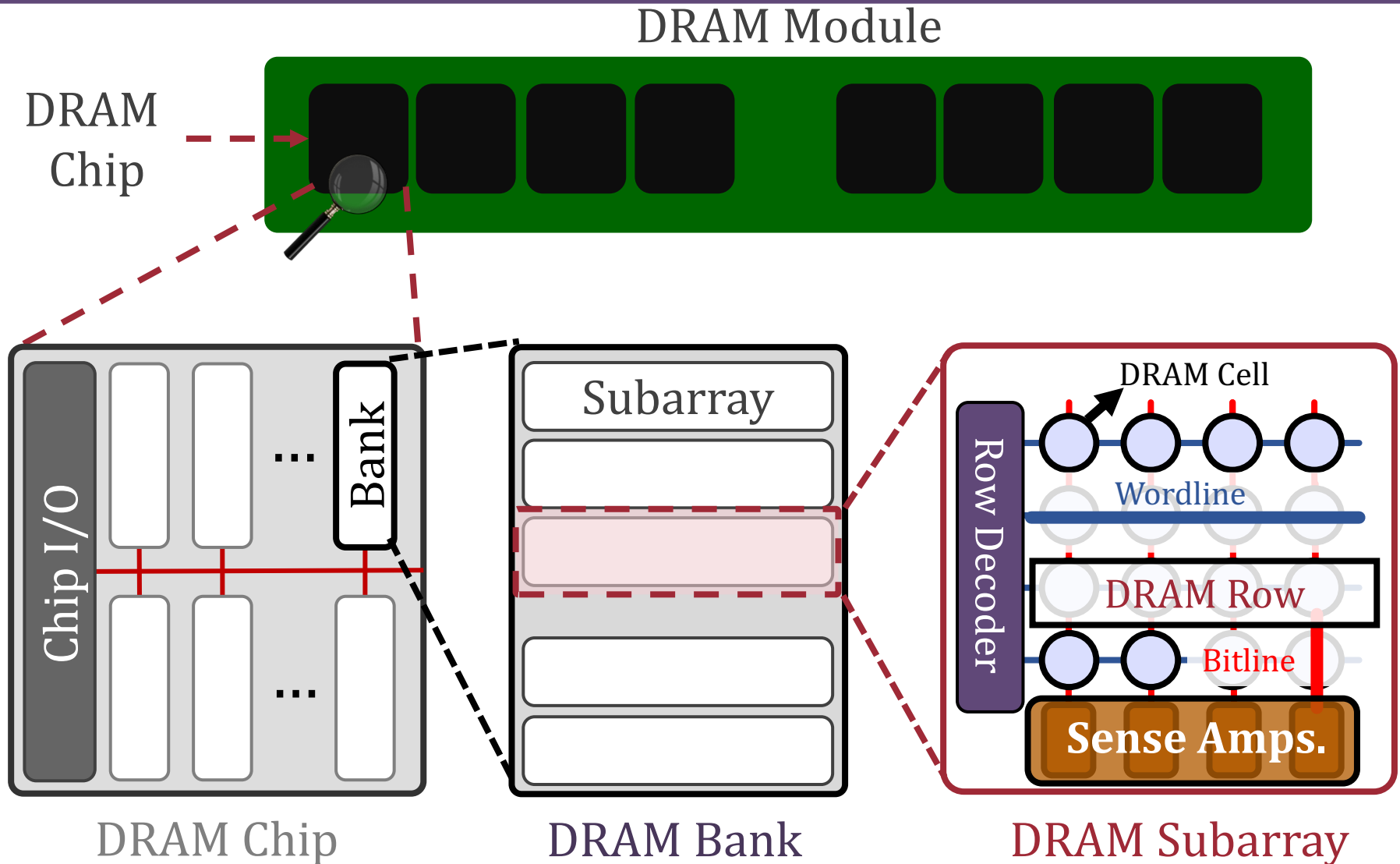
Real DRAM Chip Results

Conclusion

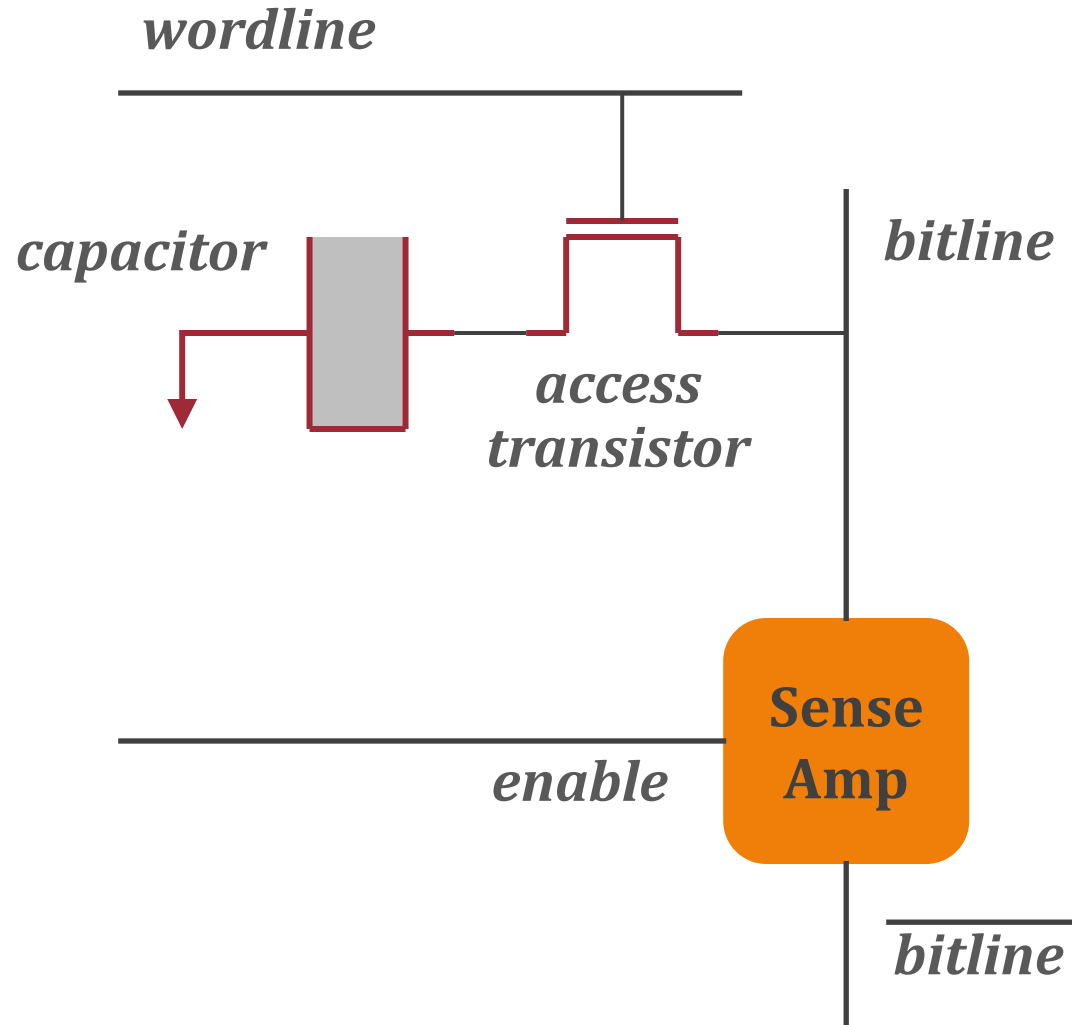
DRAM Organization



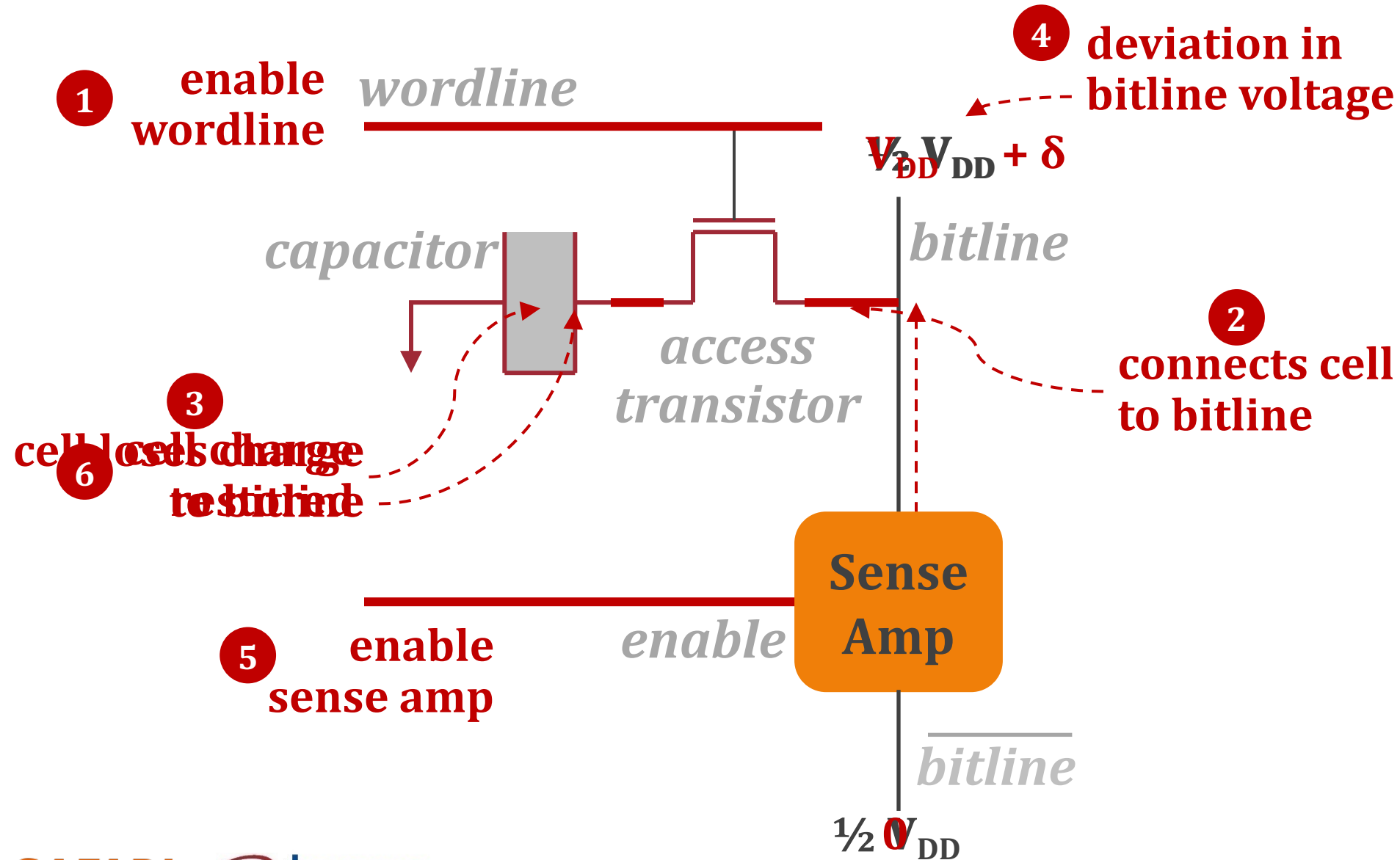
DRAM Organization



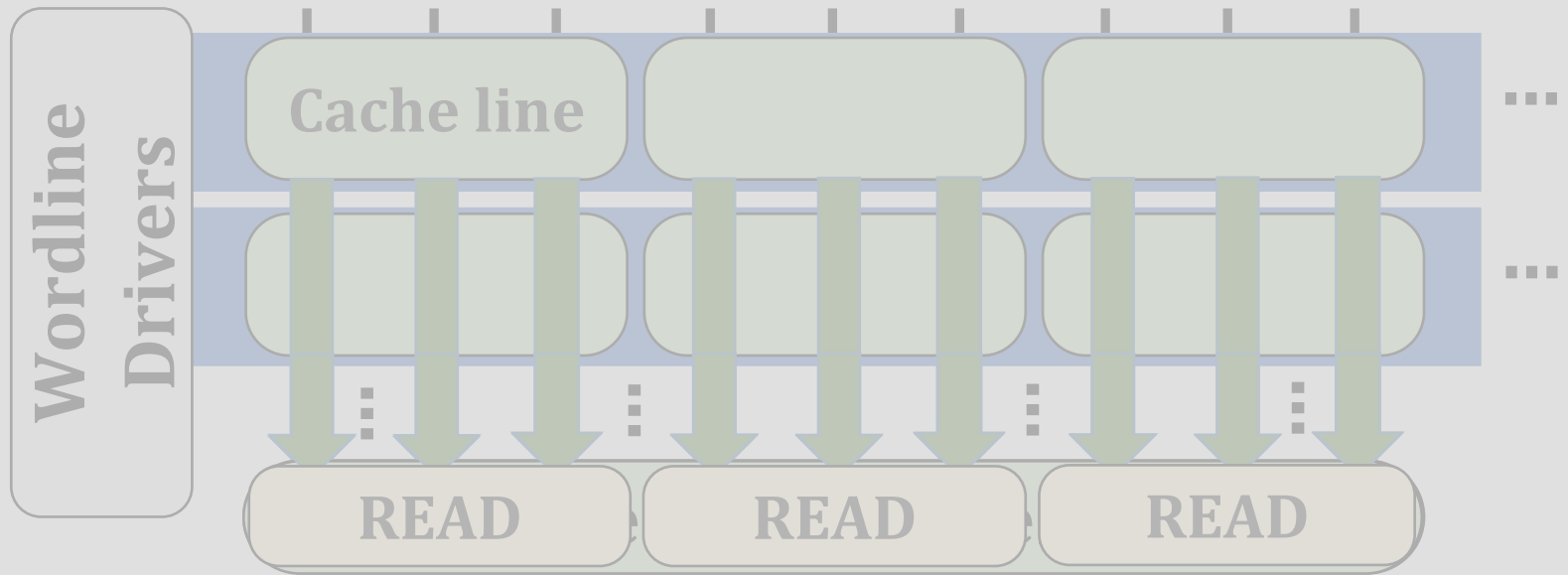
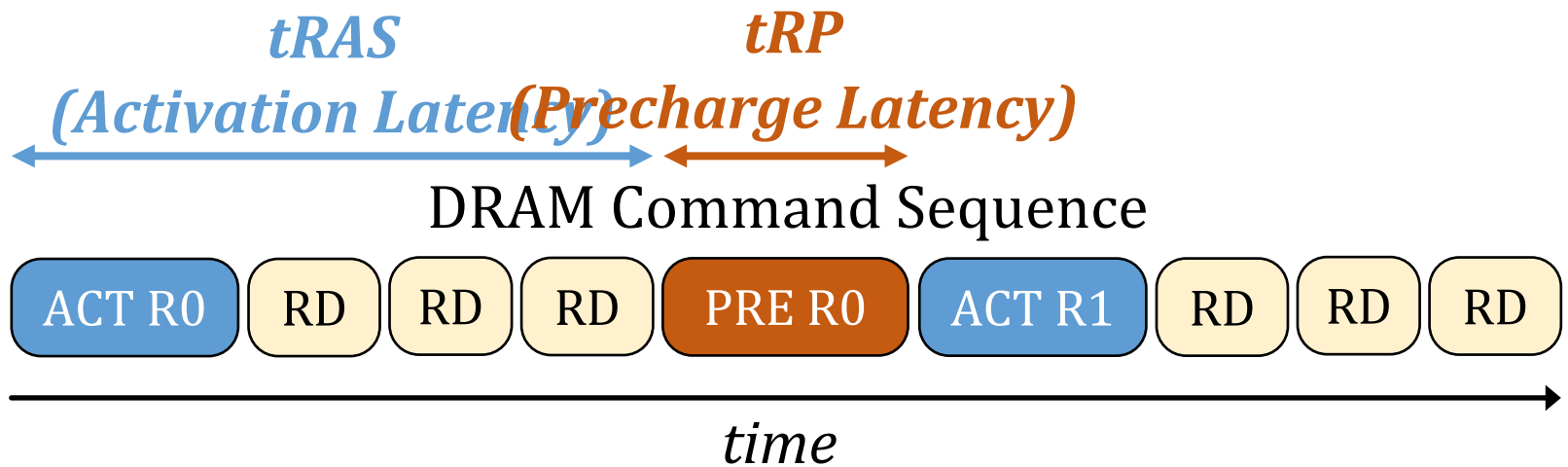
Accessing a DRAM Cell



Accessing a DRAM Cell

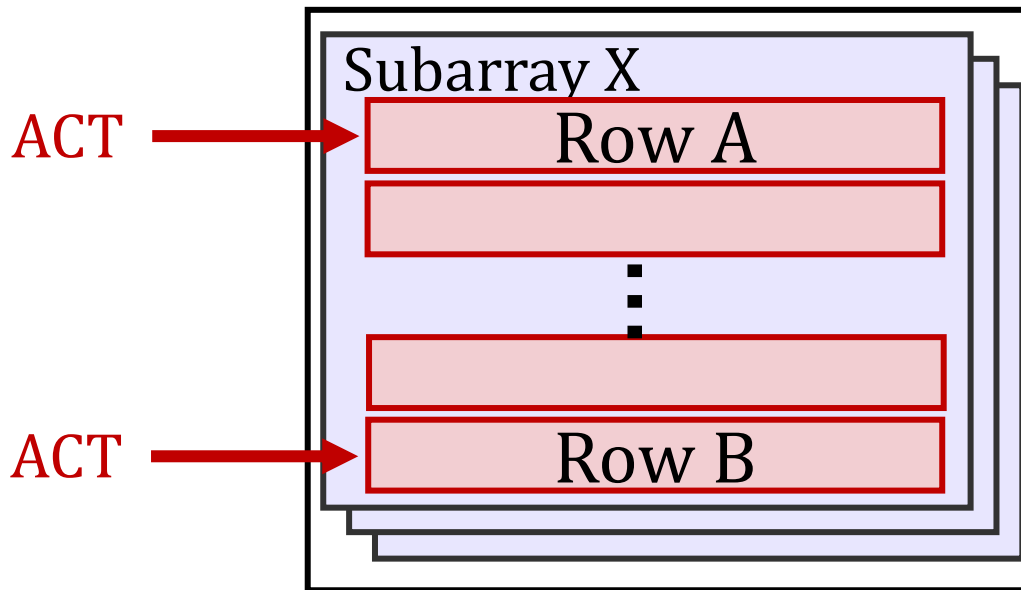


DRAM Operation



Simultaneous Multiple-Row Activation

Activating two rows in **quick succession** in **COTS** DRAM chips **simultaneously** activates **multiple rows** in a subarray



DRAM Bank

Our Goal

Experimentally understand the capability of **SiMRA** to generate **PUF responses** in **real DRAM chips**

Experimentally characterize this capability under different **designs & operating conditions**

Outline

Motivation

DRAM Organization & Operation

SiMRA-PUF

Testing Methodology

Real DRAM Chip Results

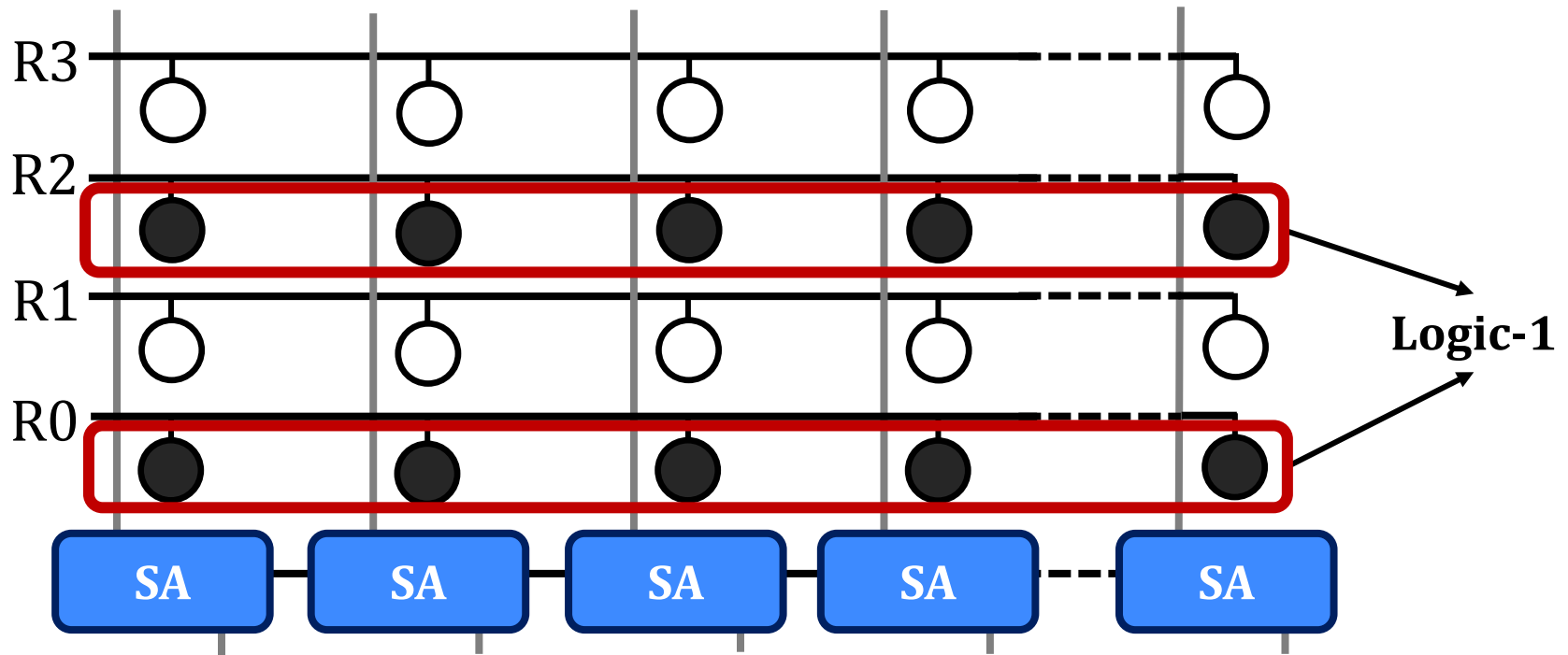
Conclusion

Key Idea

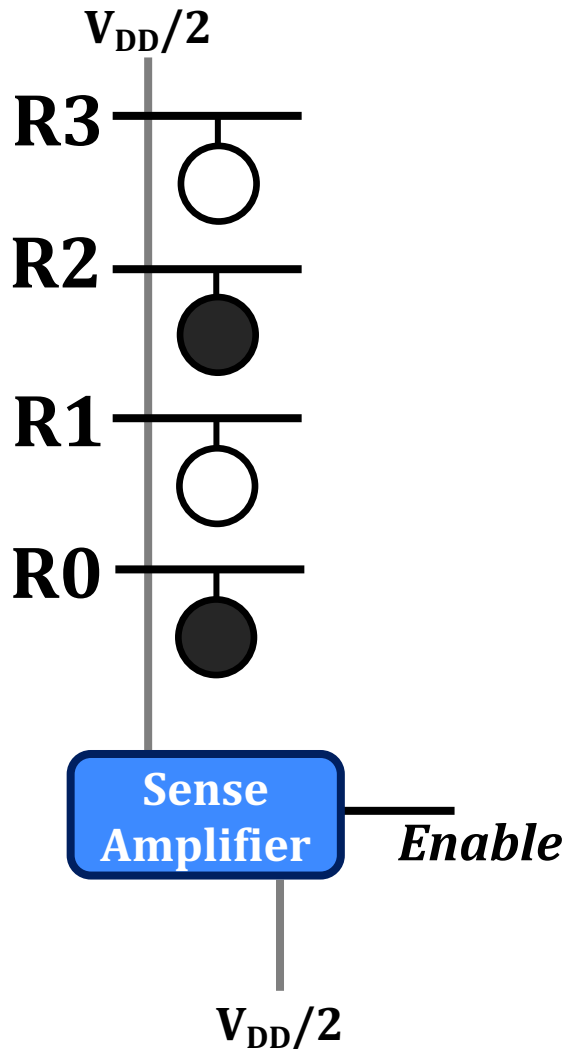
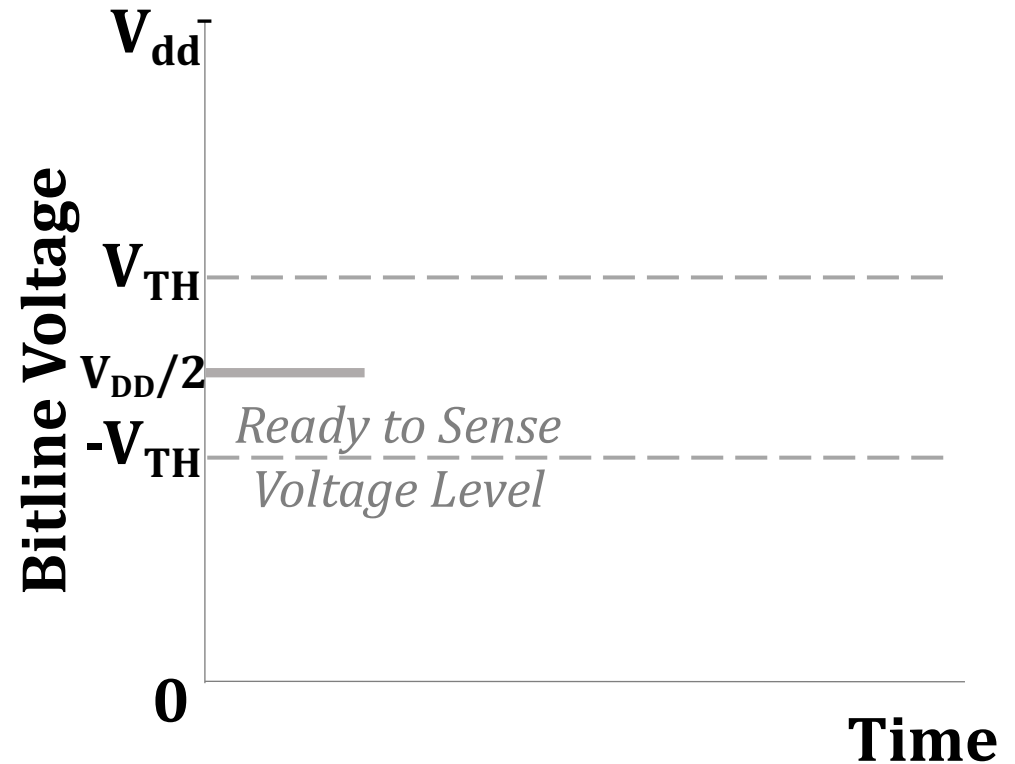
Exploit **simultaneous row activation**
to generate **device-specific signatures**

Generating Signatures via SiMRA

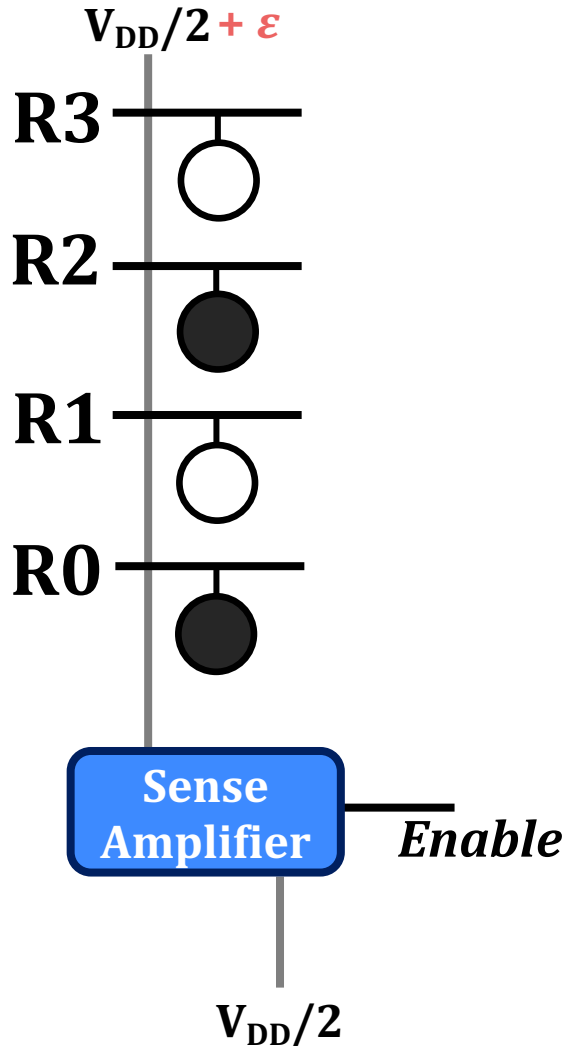
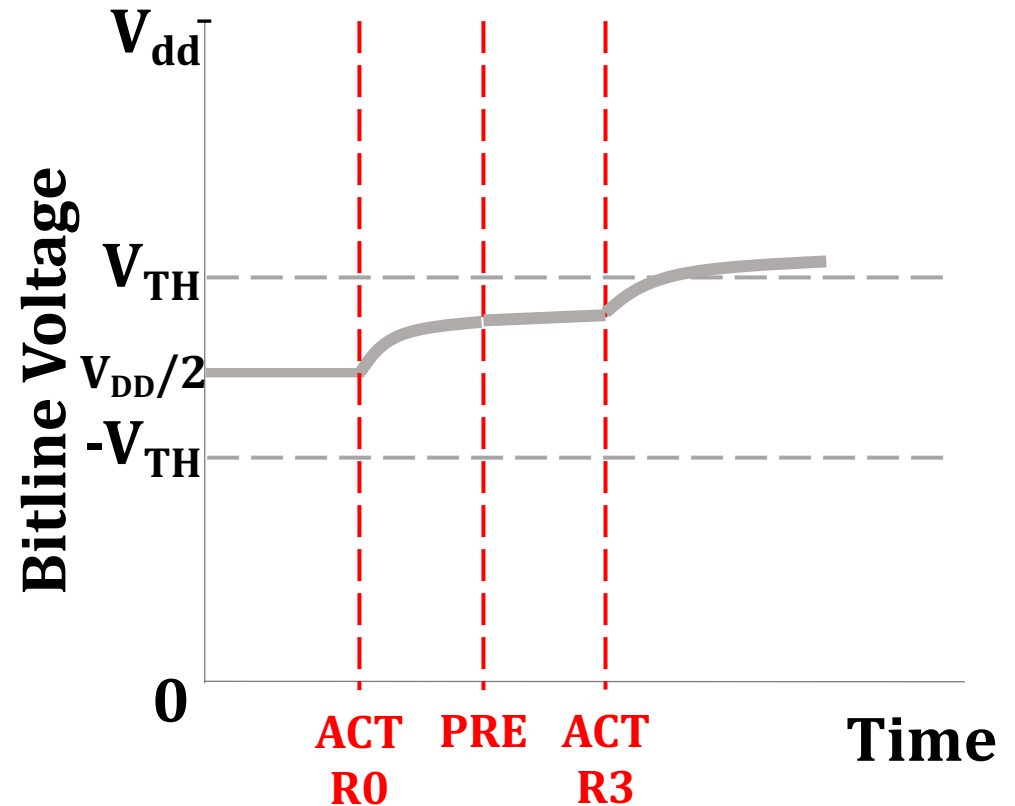
Simultaneously activate N rows with half storing **logic-1** and half storing **logic-0**



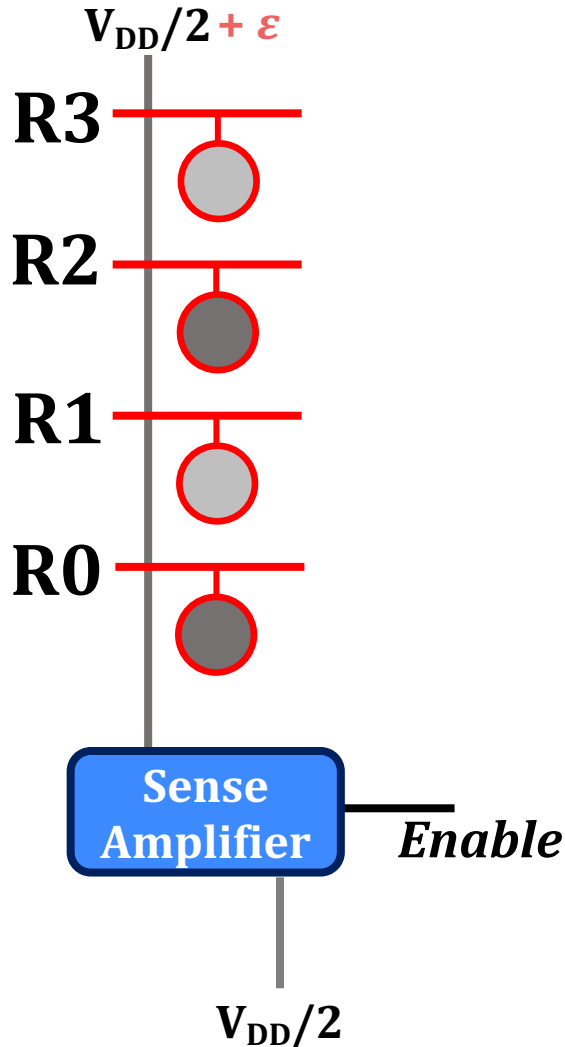
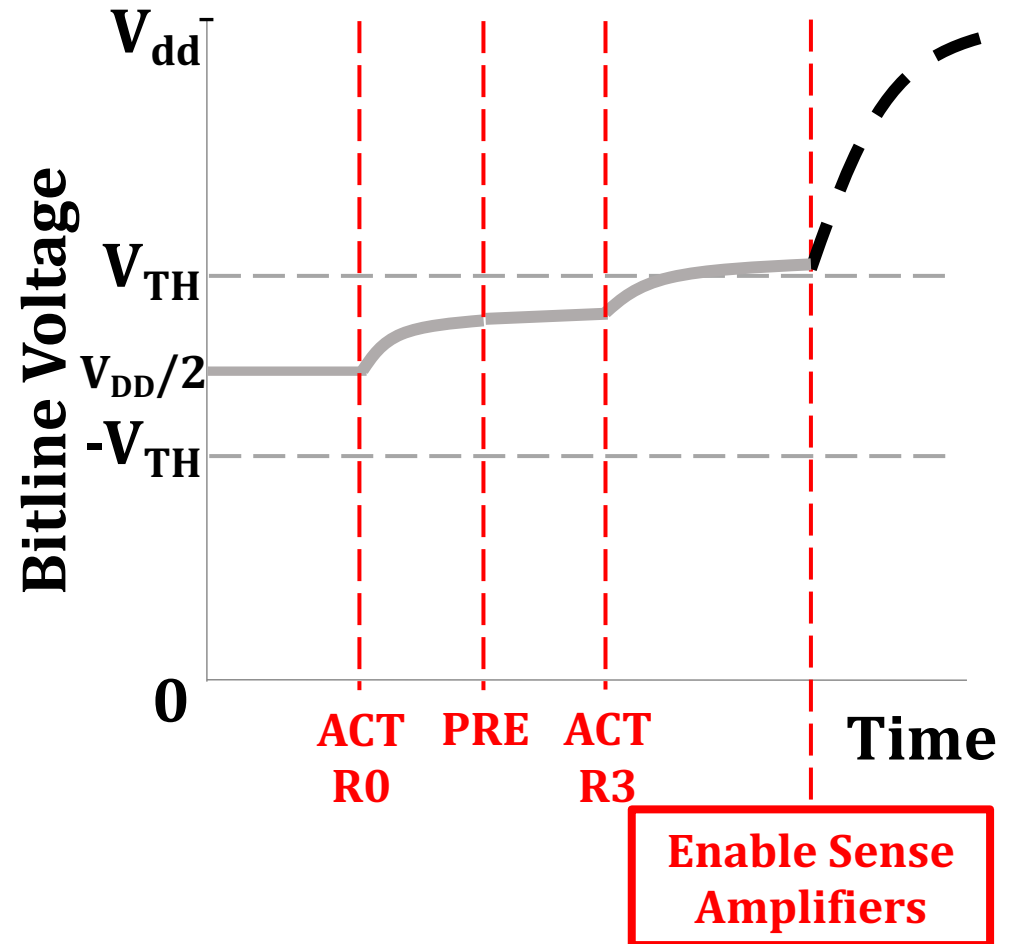
Generating Signatures via SiMRA



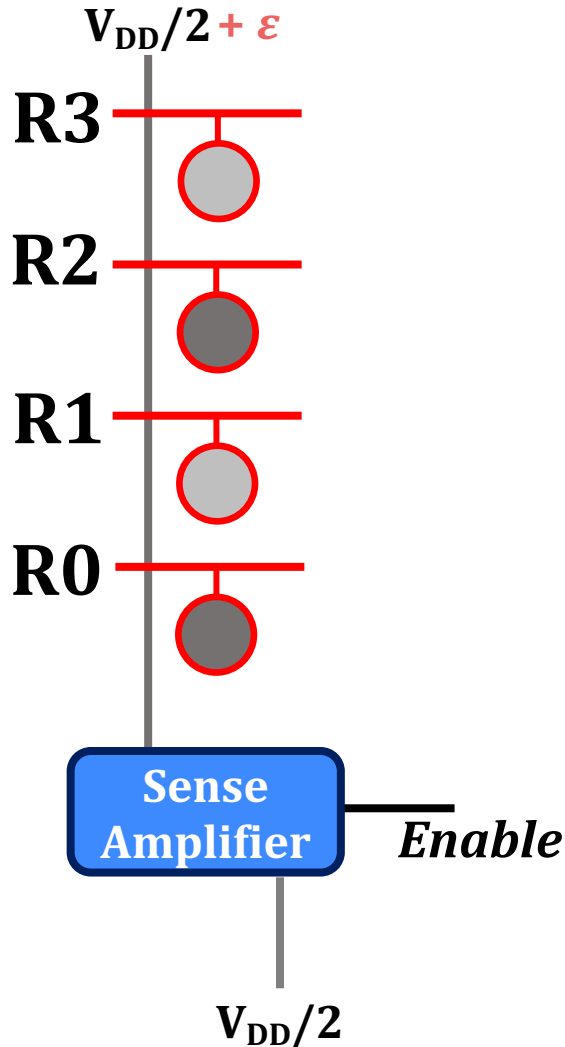
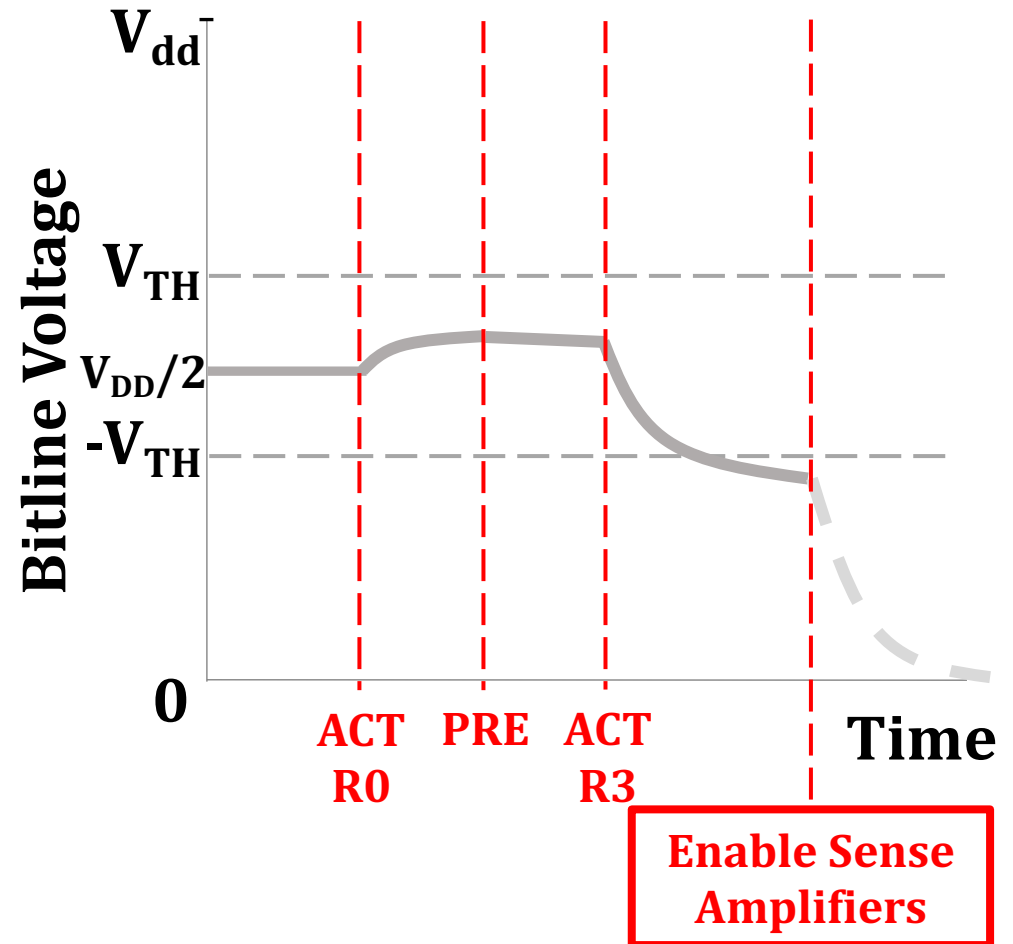
Generating Signatures via SiMRA



Generating Signatures via SiMRA



Generating Signatures via SiMRA



SiMRA-PUF Designs

Number of simultaneously activated rows:

- 2/4/8/16/32

Challenge-Response Definition:

- Challenge = $(\text{Bank}_{\text{ID}}, \text{Subarray}_{\text{ID}})$
 - One representative simultaneously activated row group (SAR) per subarray
 - One balanced data pattern per module
- Response = Signature generated by SiMRA



Outline

Motivation

DRAM Organization & Operation

SiMRA-PUF

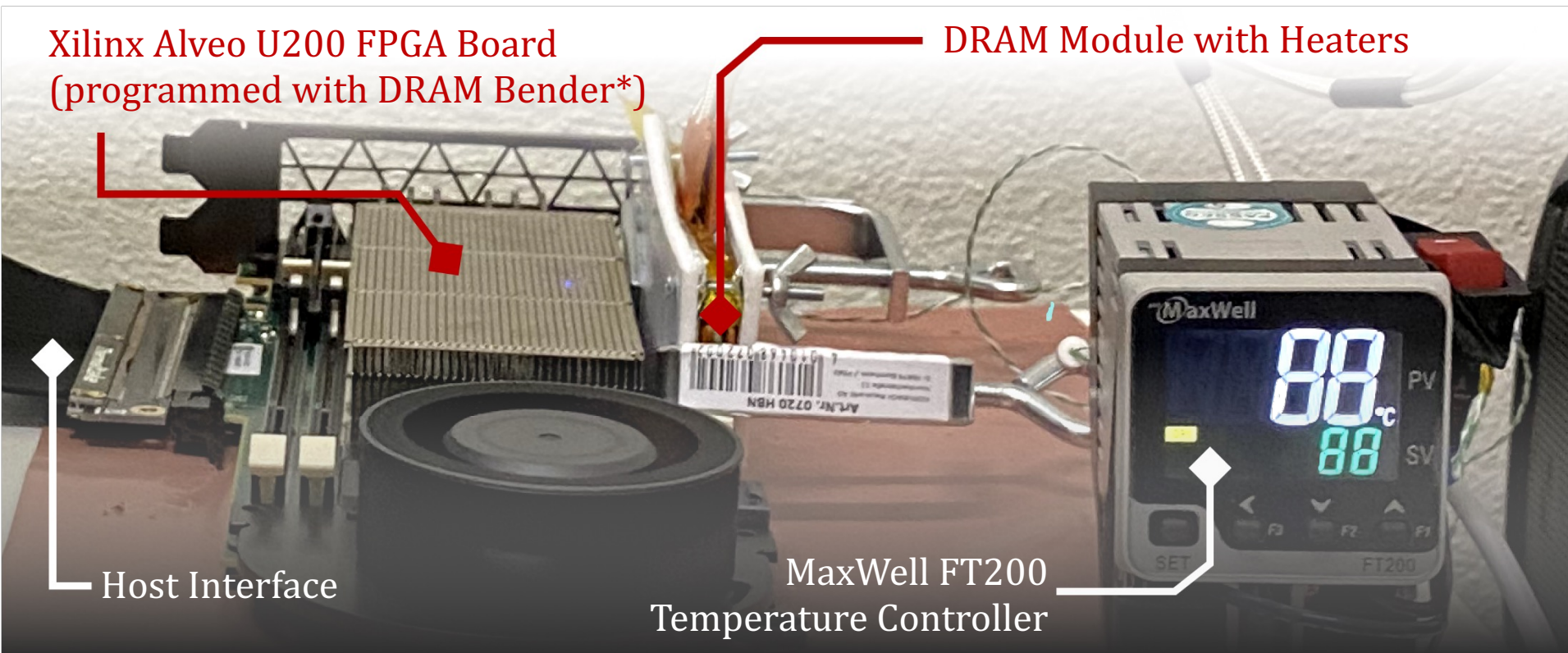
Testing Methodology

Real DRAM Chip Results

Conclusion

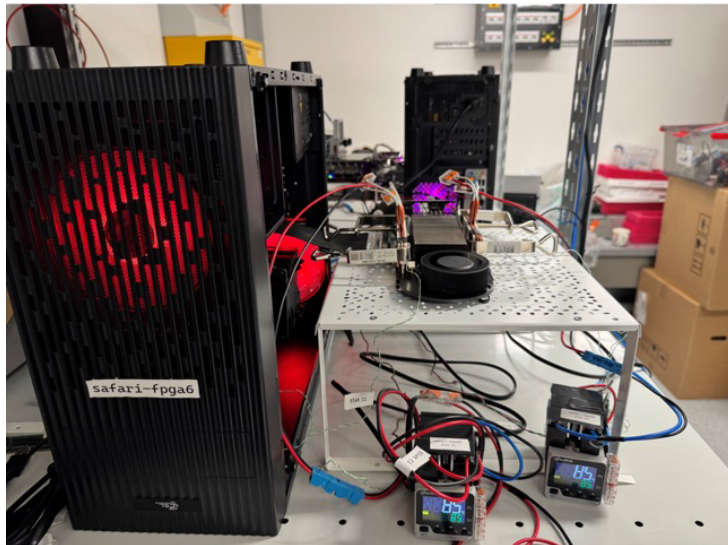
DDR4 DRAM Testing Infrastructure

DRAM Bender* on a Xilinx Alveo U200



Fine-grained control over **DRAM commands**,
timing parameters and **temperature**

Laboratory for Understanding Memory



*Olgun et al., arXiv, 2026

<https://arxiv.org/abs/2606.13725>

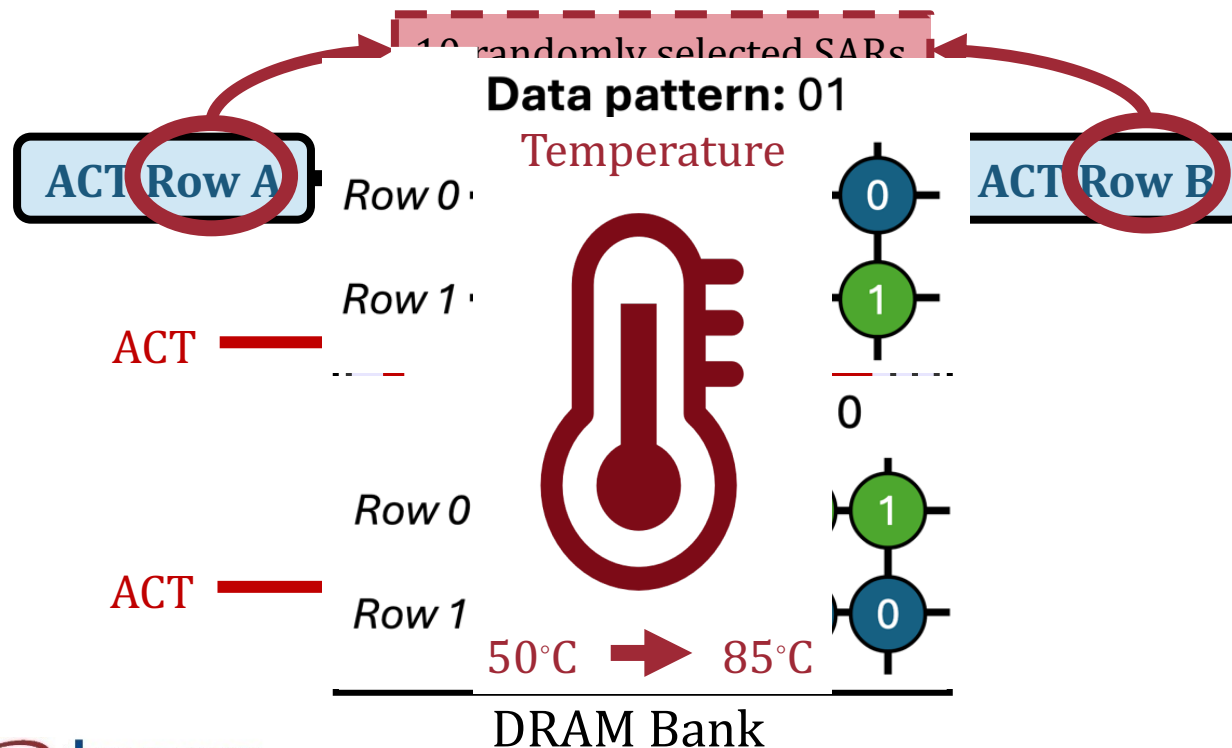
Tested DRAM Chips

- **112 real DDR4 chips** from **SK hynix**
- Covering multiple **die revisions & chip densities**

Chip Mfr.	Module Mfr.	#Modules (#Chips)	Die Rev.	Chip Density	Chip Org.	Date year-week
SK hynix	TimeTec	2 (16)	A	4Gb	x8	N/A
	SK hynix	2 (24)	A	4Gb	x8	N/A
	TeamGroup	2 (16)	M	4Gb	x8	N/A
	SK hynix	1 (8)	A	8Gb	x8	18-43
	SK hynix	2 (32)	J	8Gb	x8	N/A
	SK hynix	1 (16)	M	8Gb	x8	N/A

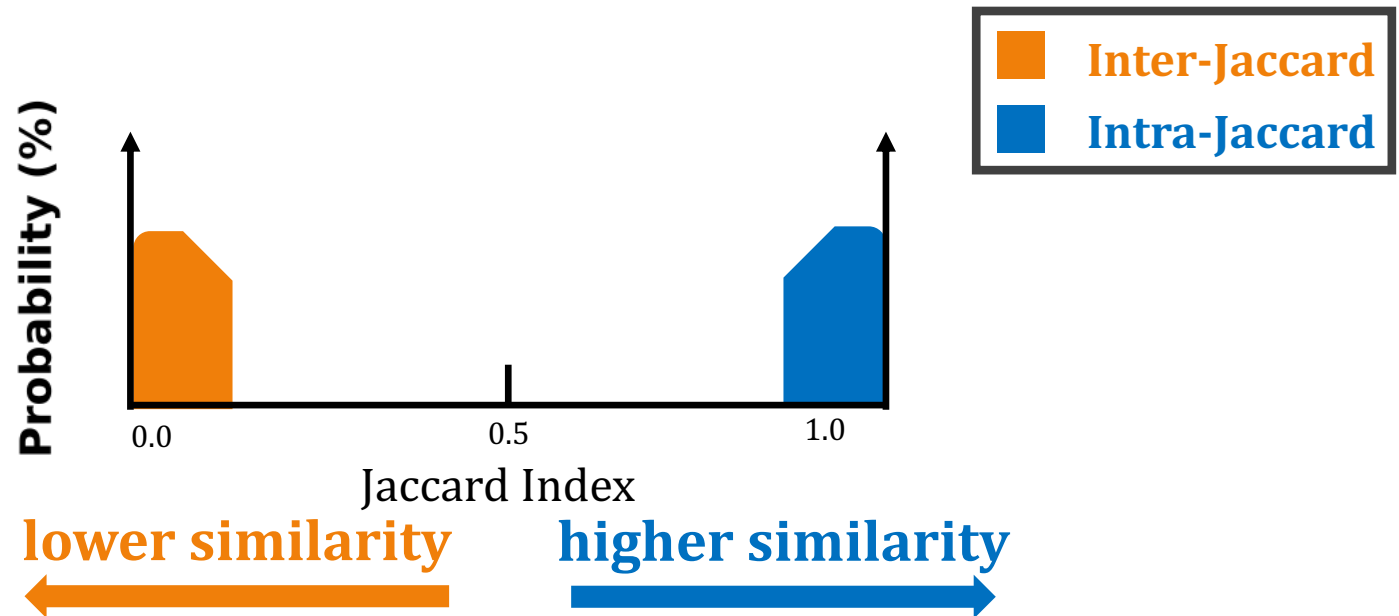
Characterization Methodology

- **Data Pattern:** Up to 100 data patterns with an equal number of all-0 and all-1 rows, for each activation count (278 in total)
- **SAR Group Selection:** Most stable SAR group within 10 randomly selected SAR groups in a subarray
- **Temperature (°C):** 50, 55, 60, 70, and 85



PUF Quality Metric

- We use **Jaccard Index** to measure the similarity of responses
 - **Uniqueness** of two responses to different challenges (**Inter-Jaccard**)
 - **Repeatability** of two responses to the same challenge (**Intra-Jaccard**)



Outline

Motivation

DRAM Organization & Operation

SiMRA-PUF

Testing Methodology

Real DRAM Chip Results

Conclusion

Major Characterization Results

Effect of Simultaneously Activated Row Count

SiMRA-PUF generates unique and repeatable responses across all numbers of simultaneously activated row counts

Effect of Chip Density & Die Revision

DRAM chip density & die revision significantly affect the uniqueness of responses

Effect of Temperature

DRAM chip temperature significantly affects the similarity of PUF responses

Major Characterization Results

Effect of Simultaneously Activated Row Count

SiMRA-PUF generates unique and repeatable responses across
all numbers of simultaneously activated row counts

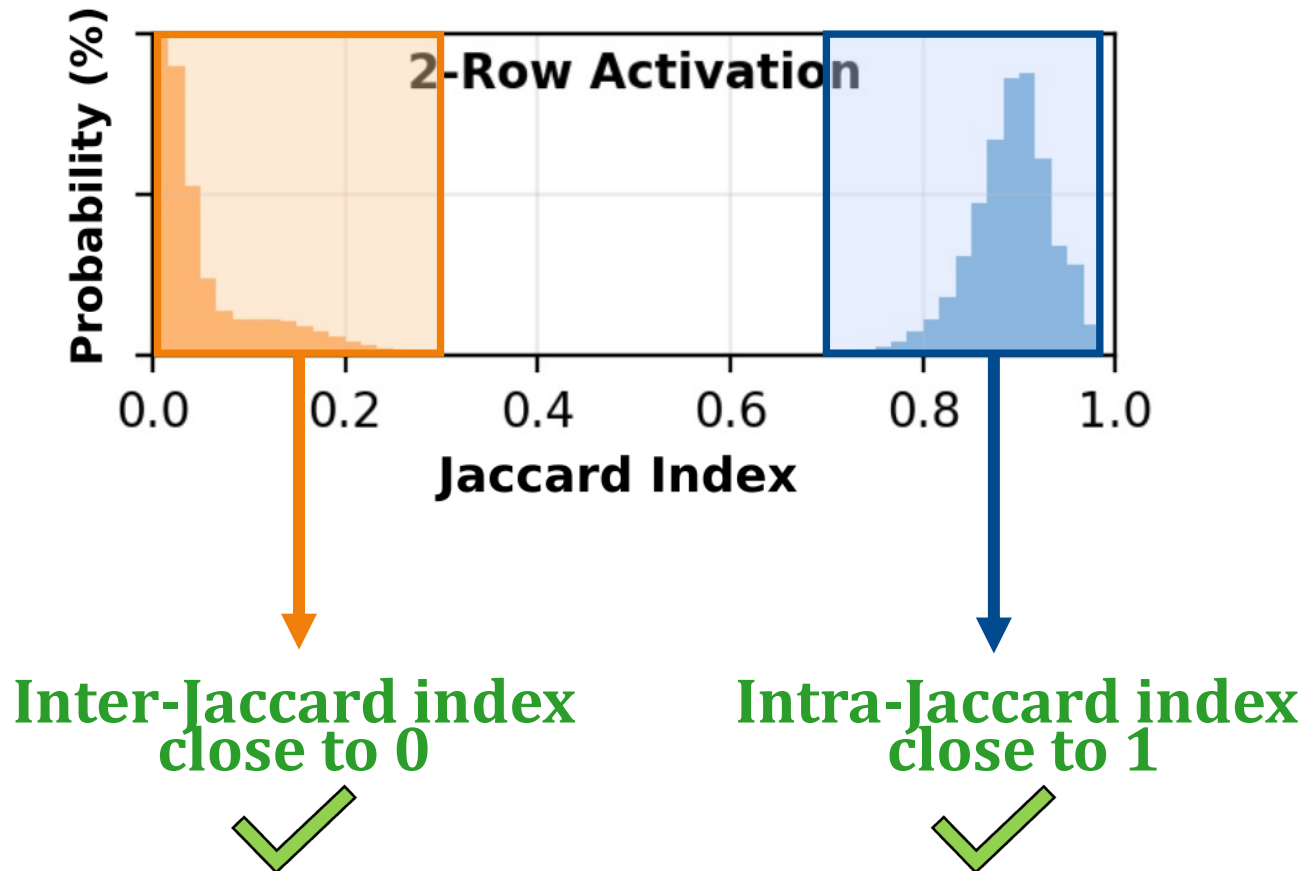
Effect of Chip Density & Die Revision

DRAM chip density & die revision significantly affect
the uniqueness of responses

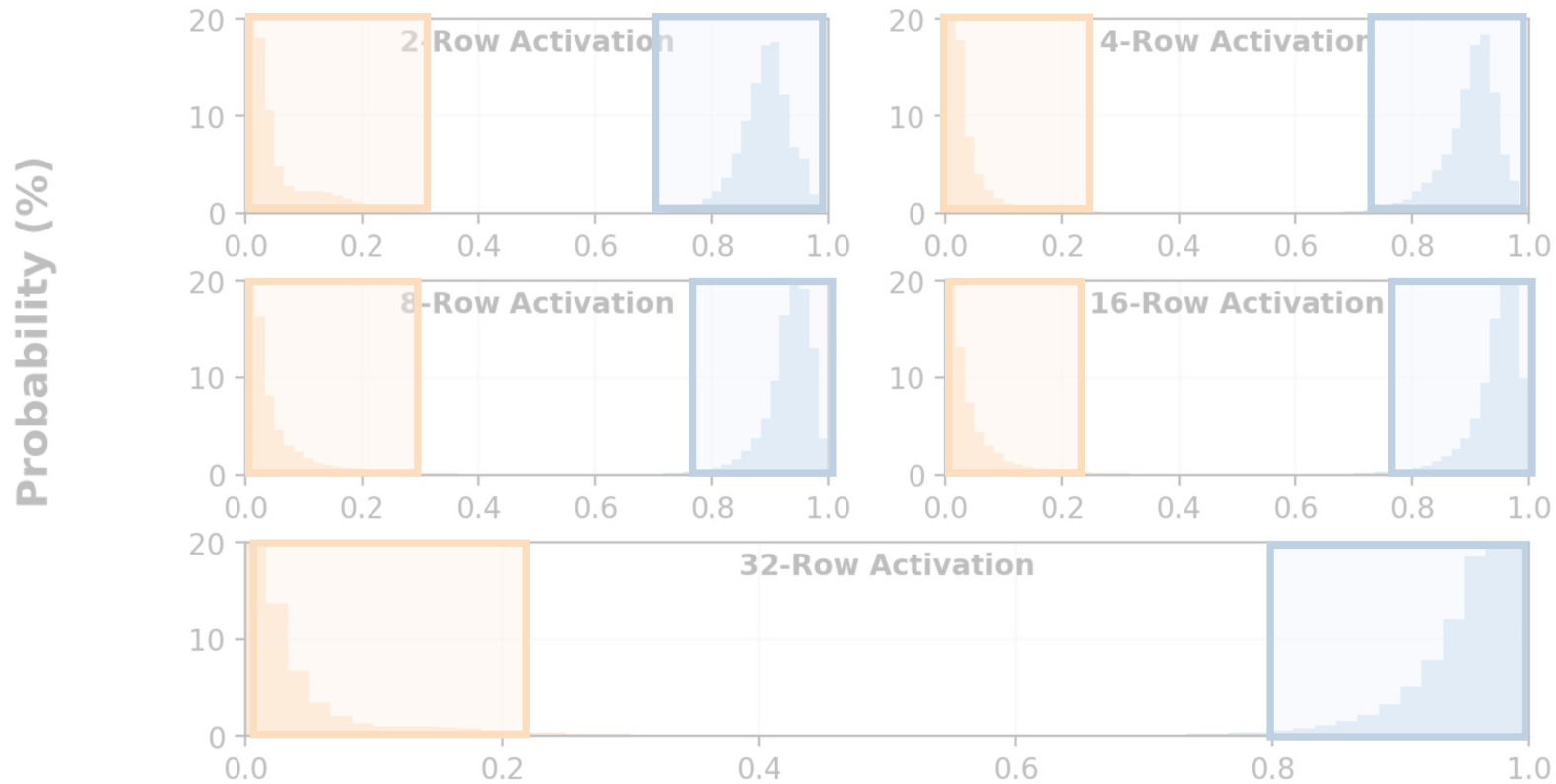
Effect of Temperature

DRAM chip temperature significantly affects
the reliability of PUF responses

Effect of Simultaneously Activated Row Count

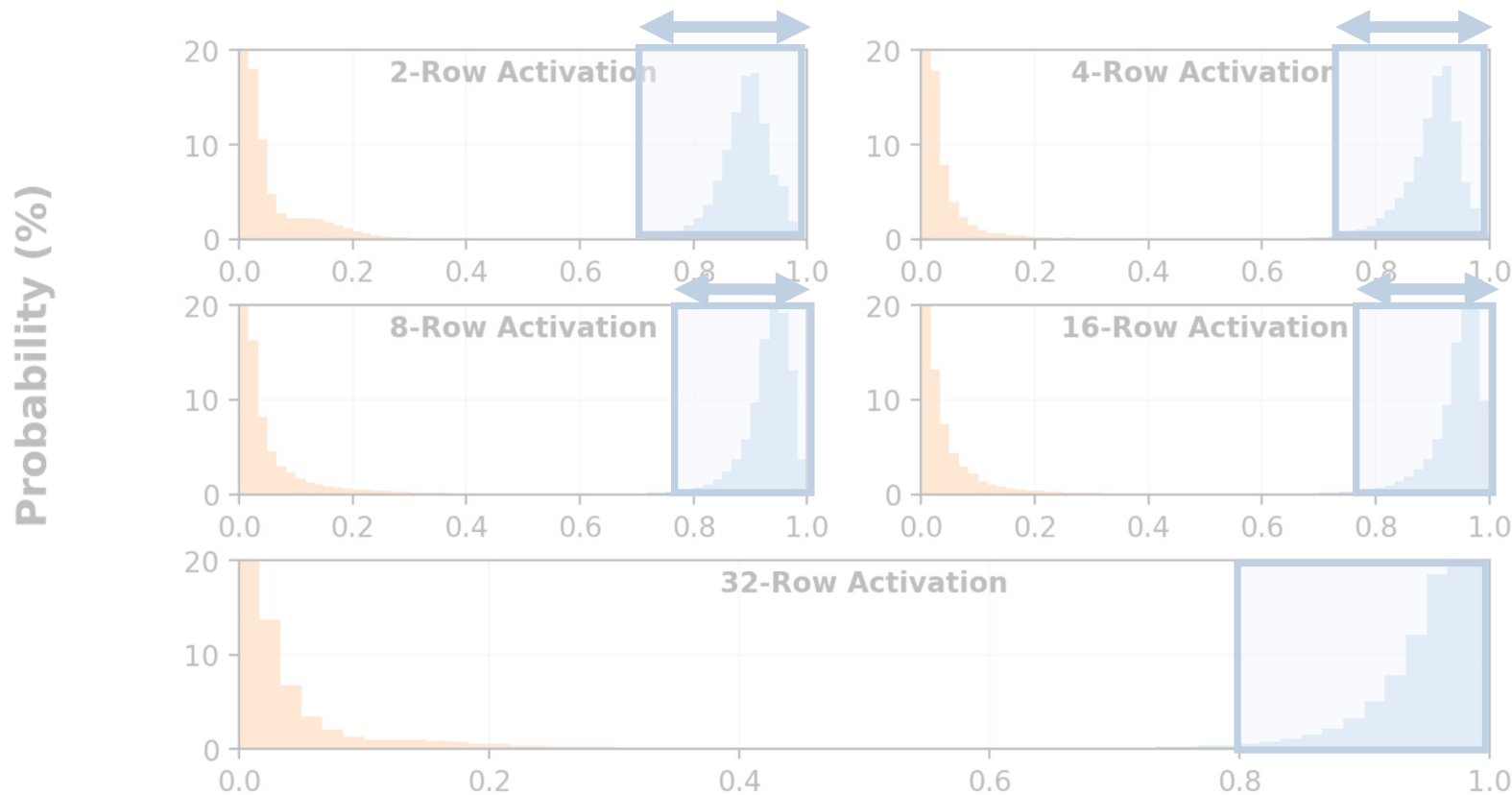


Effect of Simultaneously Activated Row Count



SiMRA-PUF generates unique and repeatable PUF responses at all tested numbers of simultaneously activated rows

Effect of Simultaneously Activated Row Count



Response **repeatability** increases as the number of simultaneously activated rows increases

Major Characterization Results

Effect of Simultaneously Activated Row Count

SiMRA-PUF generates unique and repeatable responses across all numbers of simultaneously activated row counts

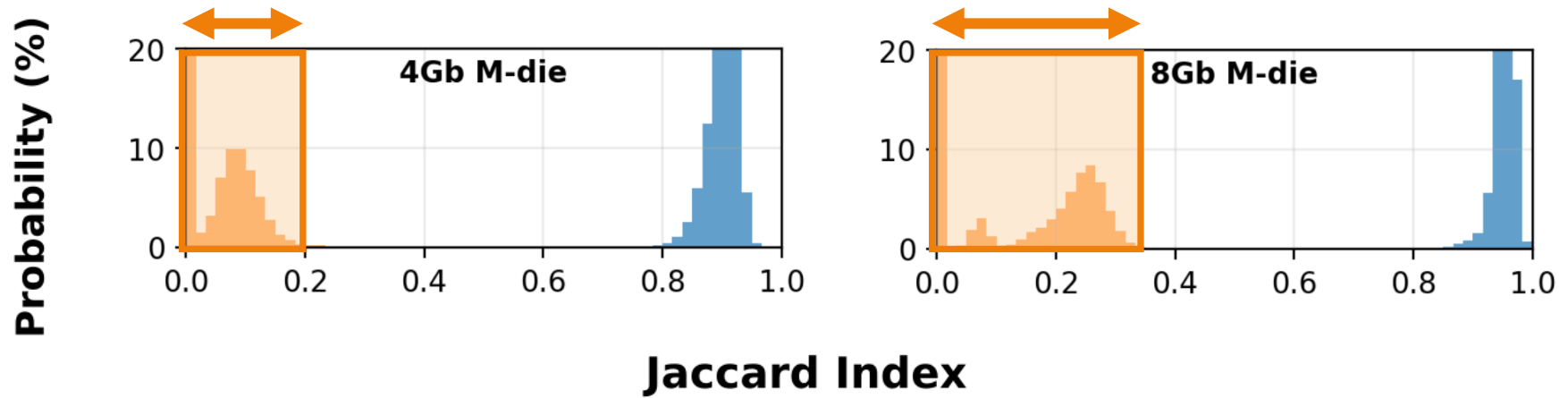
Effect of Chip Density & Die Revision

DRAM chip density & die revision significantly affect the uniqueness of responses

Effect of Temperature

DRAM chip temperature significantly affects the reliability of PUF responses

Effect of Chip Density & Die Revision



DRAM chip density & die revision **significantly** affect the similarity of responses to different challenges

Major Characterization Results

Effect of Simultaneously Activated Row Count

SiMRA-PUF generates unique and repeatable responses across all numbers of simultaneously activated row counts

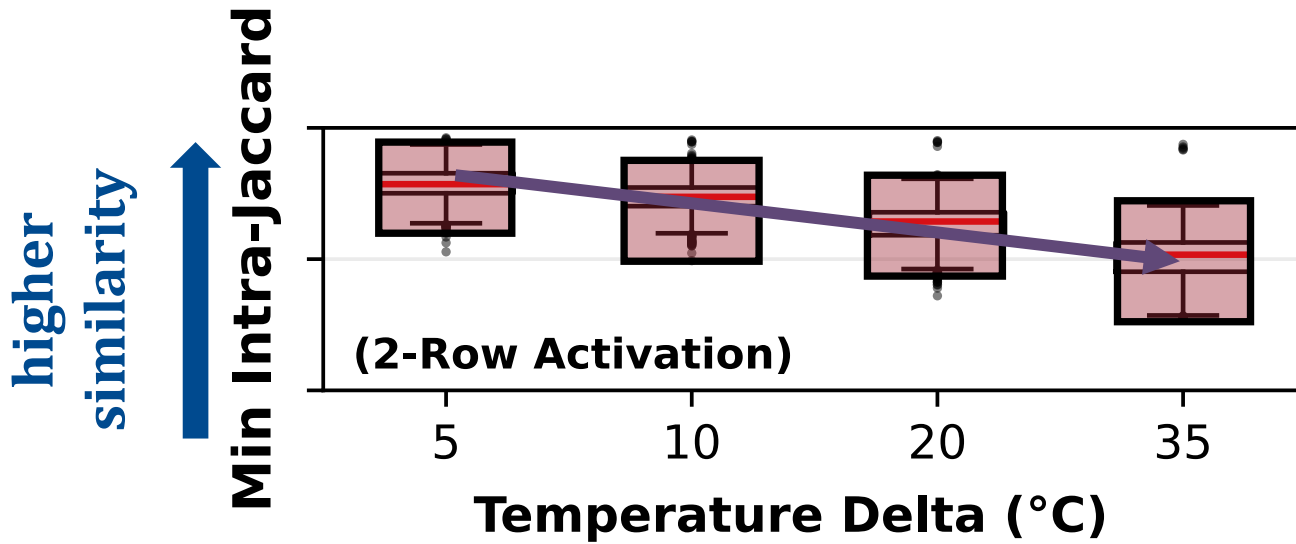
Effect of Chip Density & Die Revision

DRAM chip density & die revision significantly affect the uniqueness of responses

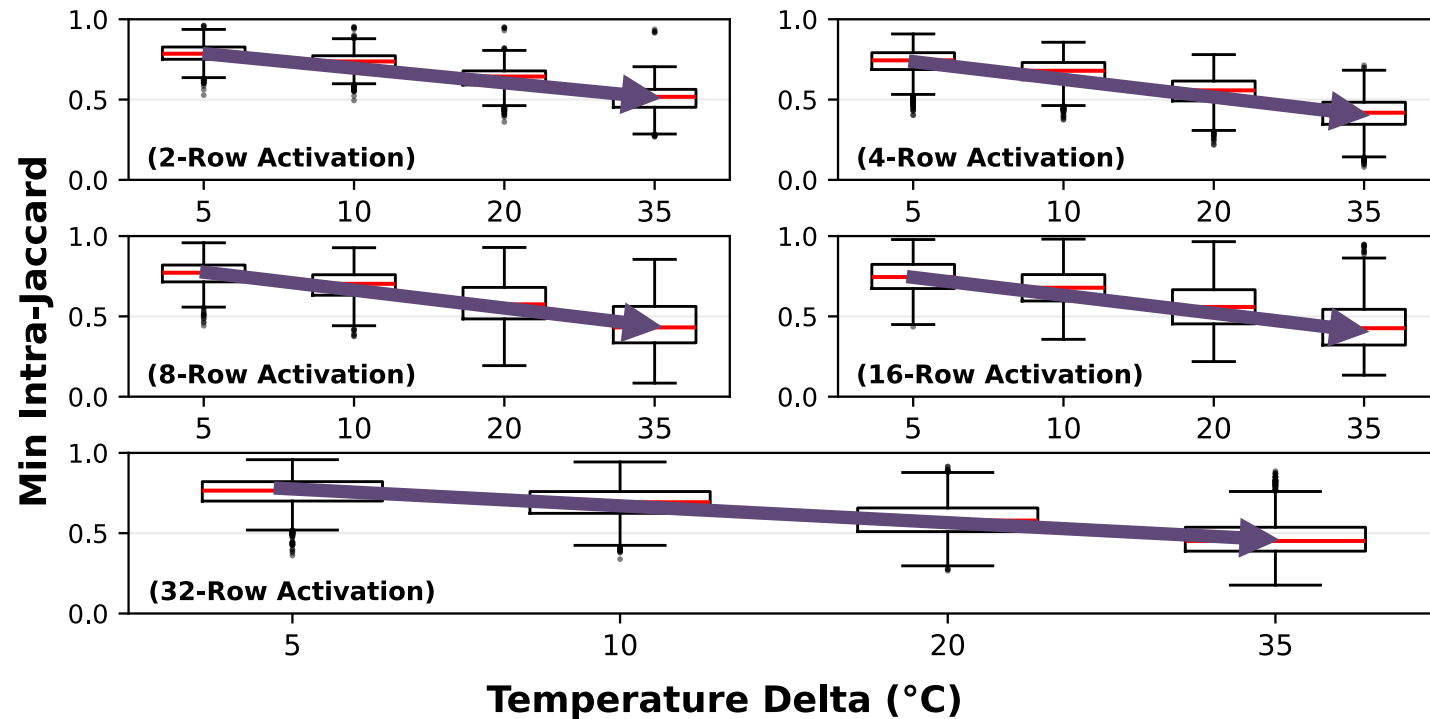
Effect of Temperature

Changes in DRAM chip temperature significantly affects the similarity of PUF responses

Effect of Temperature



Effect of Temperature



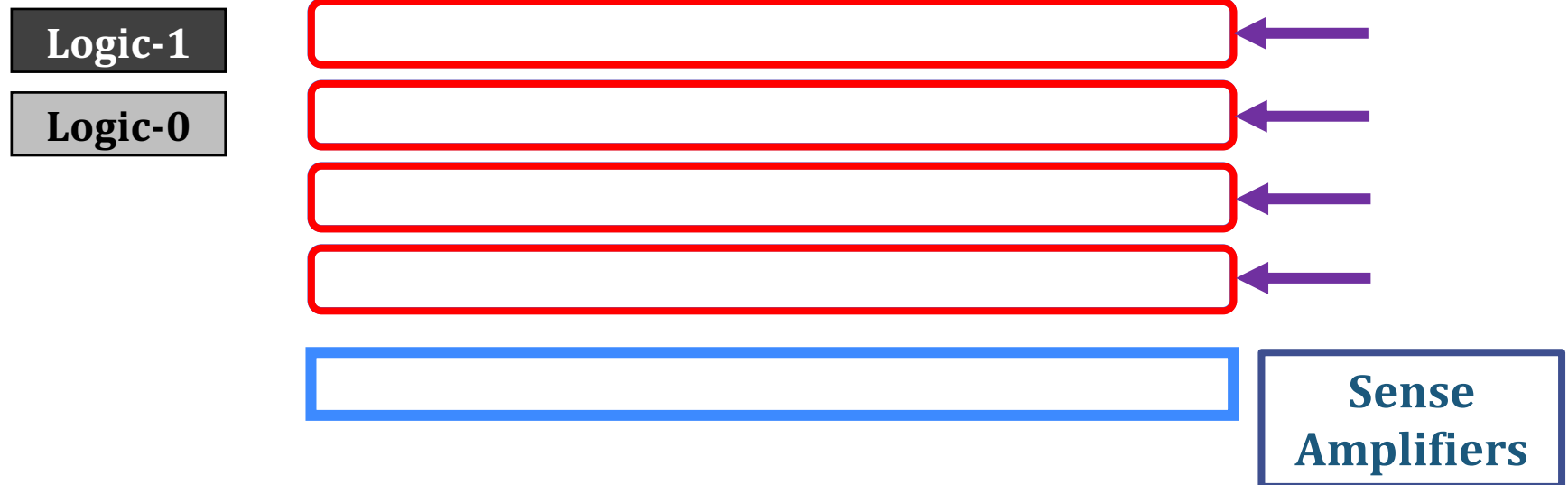
Response similarity **strictly decreases** as **temperature delta** across evaluations increases

Latency Evaluation

Measured each step of SiMRA-PUF design

- Step 1: **Initialize**
 - Perform **N RowClone* operations** for **N-row activation**

*Simultaneously
Activated Rows*



Latency Evaluation

Measured each step of SiMRA-PUF design

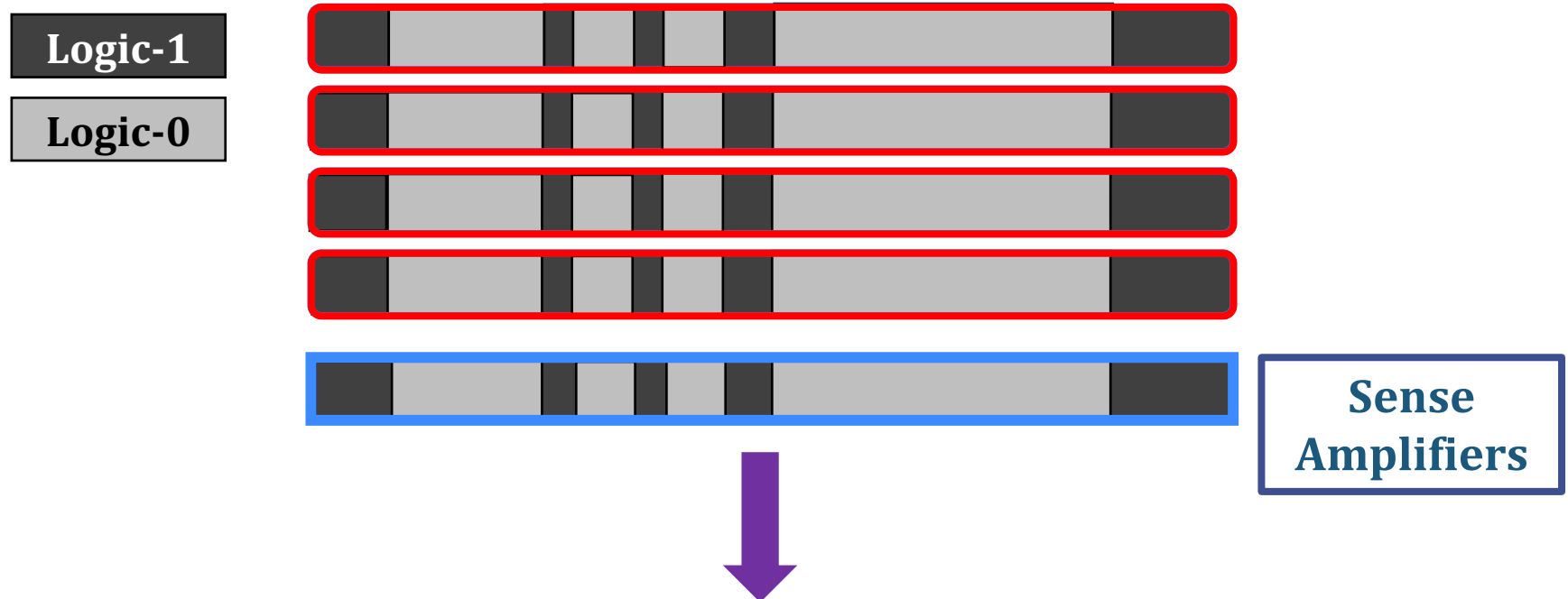
- Step 2: **SiMRA**
 - Execute **DRAM commands** that **activate N rows simultaneously** (ACT – PRE – ACT)



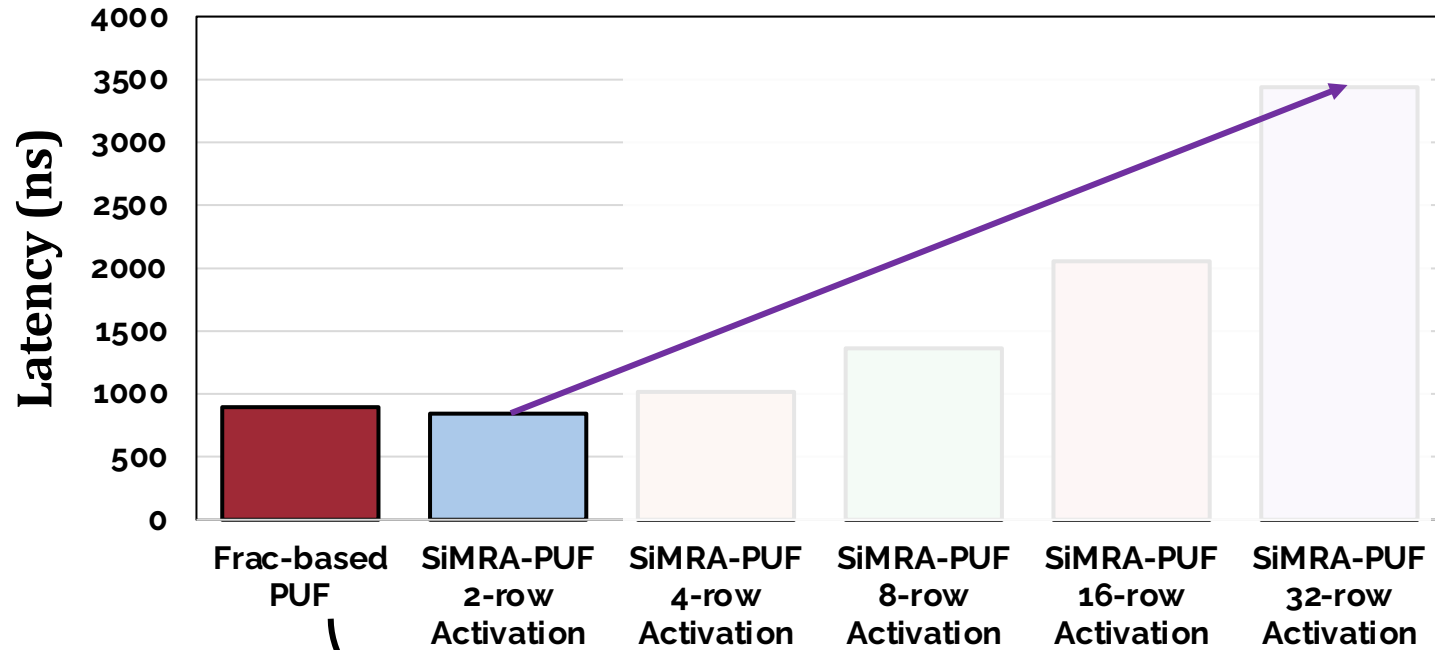
Latency Evaluation

Measured each step of SiMRA-PUF design

- Step 3: **Read**
 - Read the response from sense amplifiers



Latency Evaluation



2-row activation-based SiMRA-PUF design has 5.75% lower latency compared to state-of-the-art

Latency increases as the number of simultaneously activated rows increases

In-DRAM Signature Generation Using Simultaneous Multiple-Row Activation: An Experimental Study of Off-The-Shelf DRAM Chips

Umut Başer^{§†} İsmail Emir Yüksel[§] F. Nisa Bostancı[§] Konstantinos Sgouras[§] Ataberk Olgun[§]
Emre Hakan Demirli^{§†} Zhiheng Yue[§] Harsh Songara[§] Oğuz Ergin^{‡†} Onur Mutlu[§]

[§]ETH Zürich

[†]TOBB ETÜ

[‡]University of Sharjah

We experimentally demonstrate that it is possible to generate unique repeatable, and device-specific signatures suitable for use as Physical Unclonable Function (PUF) responses in commercial off-the-shelf (COTS) DRAM chips by leveraging simultaneous multiple-row activation (SiMRA). Based on a rigorous experimental characterization of 112 modern DDR4 DRAM chips (from 10 modules), we introduce SiMRA-PUF, the first DRAM-based PUF that uses SiMRA-generated signatures as PUF responses. We analyze SiMRA-PUF in terms of reliability, uniqueness, and evaluation latency for varying numbers of simultaneously activated DRAM rows (i.e., 2, 4, 8, 16, and 32), DRAM chip density & die revision, and evaluate how temperature affects the similarity of SiMRA-generated responses. Among our 8 key experimental observations, we highlight two major results. First, SiMRA-PUF provides average intra-Jaccard indices of 89.02%, 89.81%, 93.03%, 94.06%, and 94.86%, and average inter-Jaccard indices of 3.98%, 2.37%, 3.44%, 2.92%, and 3.24% for 2-, 4-, 8-, 16-, and 32-row activations, respectively, showing that SiMRA-generated signatures are both repeatable within a device and unique across devices. Second, 2-row activation-based SiMRA-PUF provides 5.75% lower evaluation latency than the state-of-the-art COTS DRAM-based PUF [39].

we first experimentally characterize PUF responses generated using SiMRA in 112 COTS DDR4 DRAM chips across two major parameters: 1) the number of simultaneously activated rows, and 2) DRAM chip density & revision. We analyze how temperature affects the similarity of SiMRA-generated responses. Second, we evaluate the quality of the generated PUF responses using standard PUF metrics (i.e., inter- and intra-Jaccard indices [25, 26, 32, 33, 40–42]) and evaluation latency for varying numbers of simultaneously activated rows.

Based on our extensive real DRAM chip experiments, we make eight new empirical observations. We summarize our analysis with two key findings. First, we show that SiMRA-PUF provides average intra-Jaccard indices of 89.02%, 89.81%, 93.03%, 94.06%, and 94.86%, and average inter-Jaccard indices of 3.98%, 2.37%, 3.44%, 2.92%, and 3.24% for 2-, 4-, 8-, 16-, and 32-row activations, respectively. Second, the 2-row activation-based SiMRA-PUF leads to 5.75% lower evaluation latency than the state-of-the-art COTS DRAM-based PUF [39]. These results demonstrate that SiMRA-PUF can be used as a fast, low-overhead PUF on real COTS DRAM chips.

We make the following contributions:

<https://arxiv.org/pdf/2606.15470>

Outline

Motivation

DRAM Organization & Operation

SiMRA-PUF

Testing Methodology

Real DRAM Chip Results

Conclusion

Conclusion

We experimentally demonstrate the potential of **simultaneous multiple-row activation (SiMRA)** to generate PUF responses

We characterize 112 off-the-shelf DDR4 DRAM chips

- DRAM chip density & die revision significantly affect the uniqueness of responses
- Increase in the temperature difference between evaluations degrades response similarity

- SiMRA-PUF provides **unique, repeatable, and fast** PUF responses
- **5.75% lower evaluation latency** compared to the **state-of-the-art** DRAM-based PUF

In-DRAM Signature Generation Using Simultaneous Multiple-Row Activation

An Experimental Study of Off-The-Shelf DRAM Chips

Umut Başer

İsmail Emir Yüksel F. Nisa Bostancı Konstantinos Sgouras

Ataberk Olgun Emre H. Demirli Zhiheng Yue Harsh Songara

Oğuz Ergin Onur Mutlu

SAFARI

ETH zürich

 **kasirga**



TOBB ETÜ
University of Economics & Technology

In-DRAM Signature Generation Using Simultaneous Multiple-Row Activation

An Experimental Study of Off-The-Shelf DRAM Chips

Backup Slides

Umut Başer

İsmail Emir Yüksel F. Nisa Bostancı Konstantinos Sgouras

Ataberk Olgun Emre H. Demirli Zhiheng Yue Harsh Songara

Oğuz Ergin Onur Mutlu

SAFARI

ETH zürich

 **kasirga**

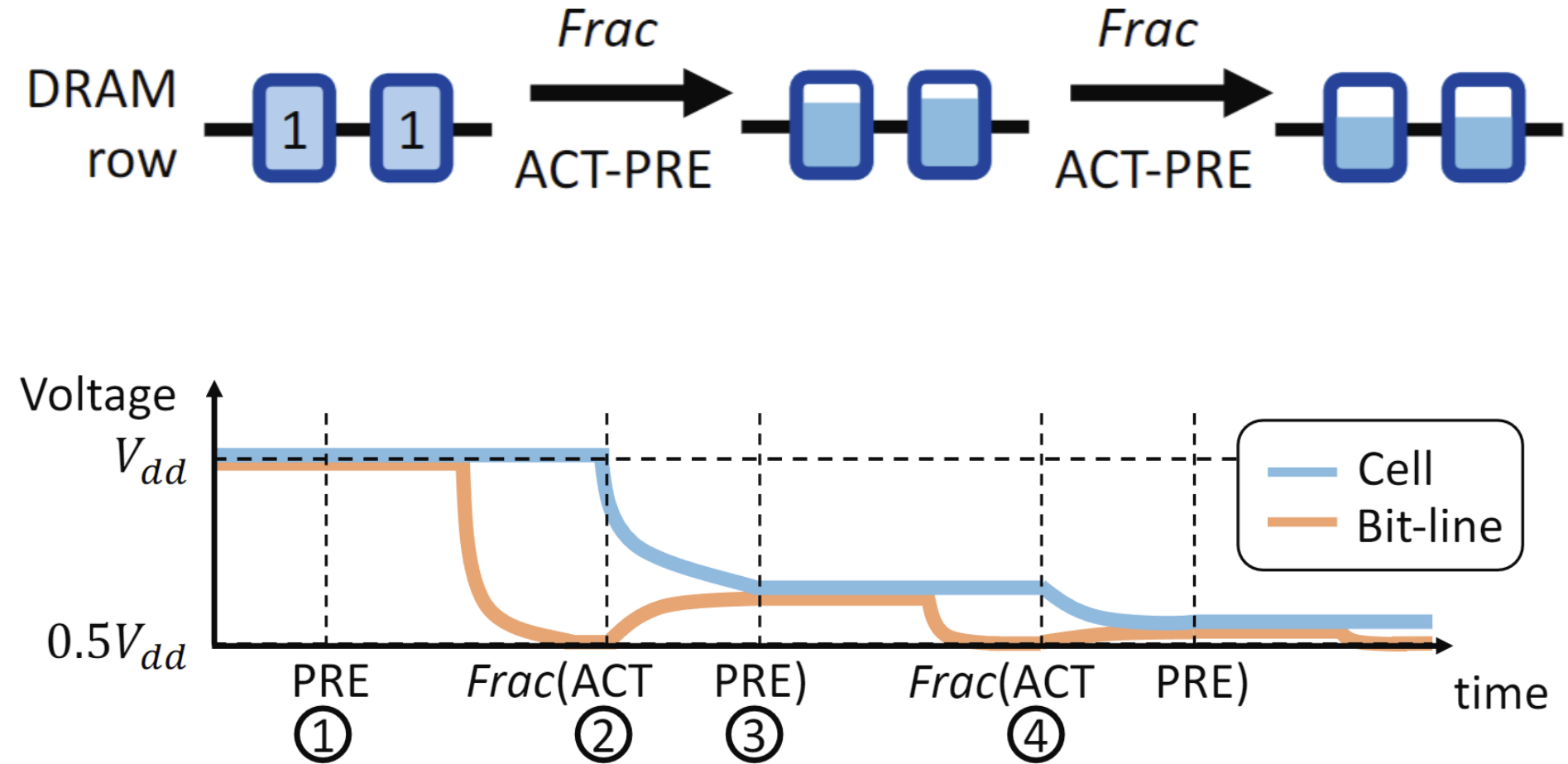


TOBB ETÜ
University of Economics & Technology

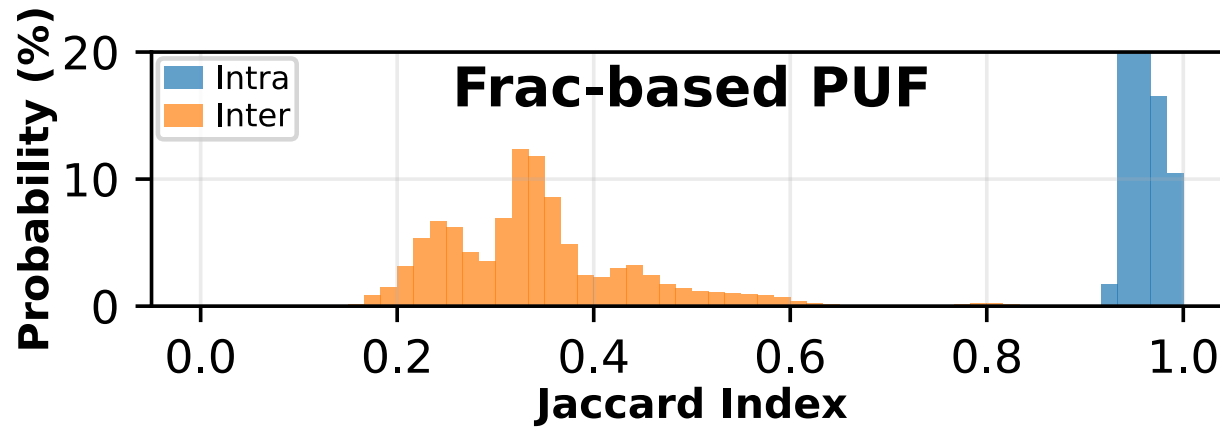
Future Work

- Understand the sources of similarities between different challenges on the same device
- Enable the use of multiple SAR groups within a single subarray to expand the challenge-response space
- Test more DRAM chips

Frac-based PUF



Frac-based PUF Results



Tested DRAM Modules

Detailed characteristics and per-module SiMRA-PUF Response Quality

DRAM Mfr.	Module Mfr.	Die Density (Gb)	Die Rev.	DQ	Frequency (MT/s)	DRAM Part	DIMM Part	DIMM Date Code
SK hynix	TimeTec	4	A	x8	2133	H5AN4G8NAFR-TFC	Unknown	Unknown
SK hynix	TimeTec	4	A	x8	2133	H5AN4G8NAFR-TFC	75TT21NUS1R8-4	Unknown
SK hynix	SK hynix	4	A	x8	2133	Unknown	HMA41GU6AFR8N-TF [1]	17-49
SK hynix	SK hynix	4	A	x8	2133	Unknown	HMA41GU6AFR8N-TF [1]	17-49
SK hynix	TeamGroup	4	M	x8	2666	H5AN4G8NMFR-TFC	TLRD44G2666HC18F-SBK [2]	Unknown
SK hynix	TeamGroup	4	M	x8	2666	H5AN4G8NMFR-TFC	TLRD44G2666HC18F-SBK [2]	Unknown
SK hynix	SK hynix	8	A	x8	2400	H5AN8G8NAFR-UHC	HMA81GU7AFR8N-UH [3]	18-43
SK hynix	SK hynix	8	J	x8	2666	Unknown	HMA82GU6JJR8N-VK [4]	Unknown
SK hynix	TimeTec	8	J	x8	2133	H5AN8G8NJJR-VKC	Unknown	Unknown
SK hynix	SK hynix	8	M	x8	2133	Unknown	HMA82GS6MFR8N-TF [5]	Unknown

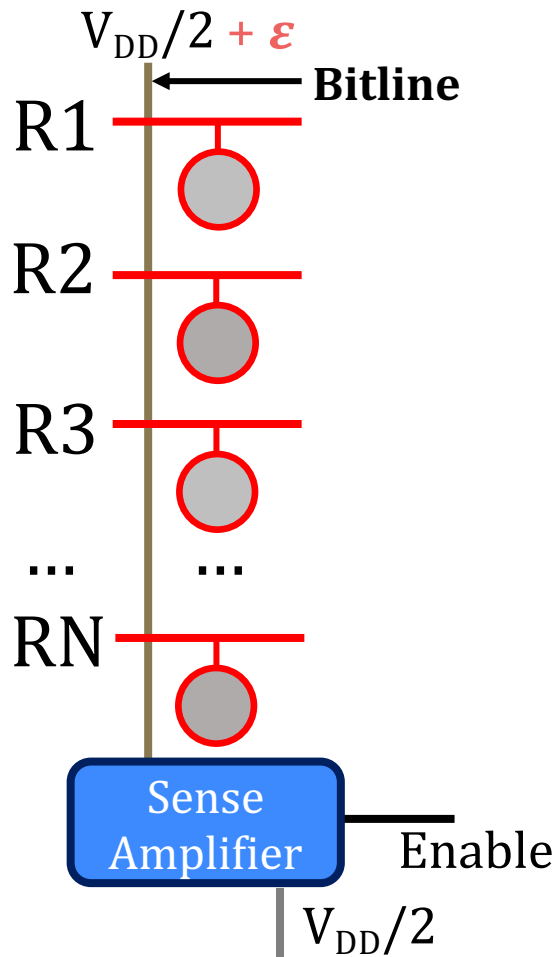
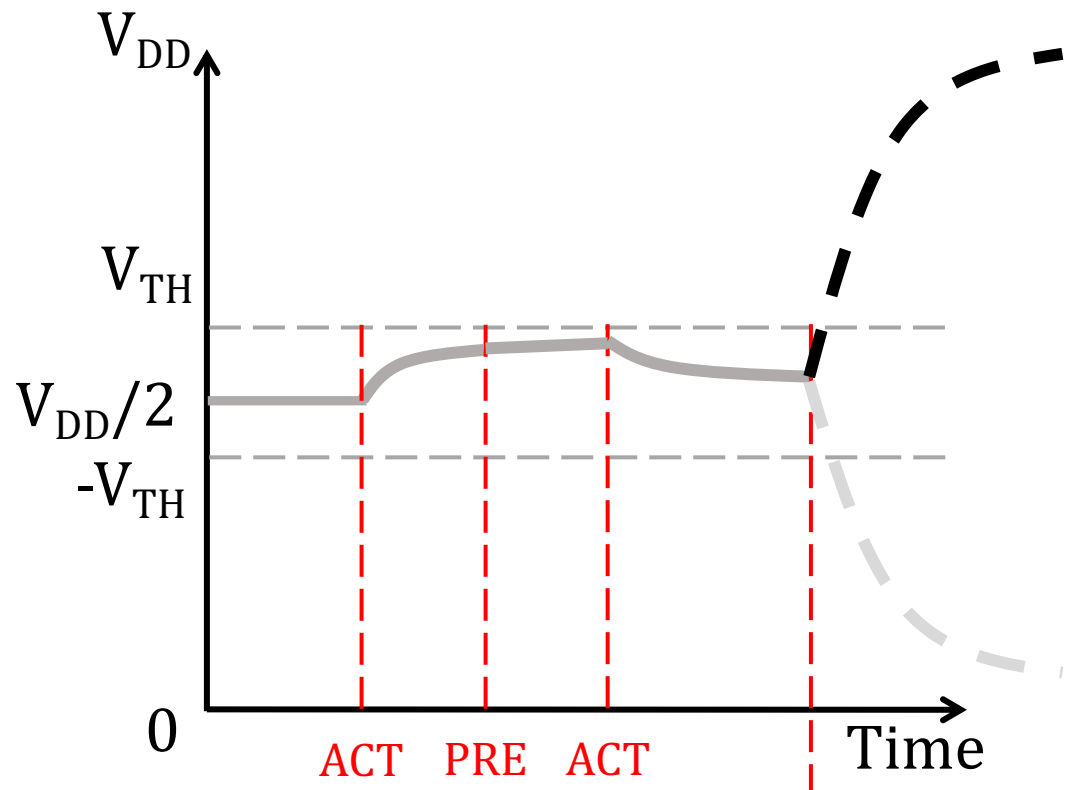
Avg. Intra-Jaccard Index (2/4/8/16/32 Row-Activation)	Avg. Intra-Jaccard Index ($\Delta T = 5/10/20/35^{\circ}\text{C}$) [†]	Avg. Inter-Jaccard Index (2/4/8/16/32 Row-Activation)		
		Intra-Bank	Inter-Bank	Inter-Module
87.40% / 89.34% / 94.01% / 95.35% / 96.36%	73.82% / 65.39% / 51.96% / 38.29%	10.07% / 7.99% / 18.74% / 13.08% / 13.00%	9.79% / 7.78% / 18.12% / 12.32% / 12.72%	3.87% / 1.99% / 2.39% / 1.99% / 2.29%
88.00% / 88.75% / 93.17% / 94.78% / 95.82%	72.71% / 64.74% / 51.65% / 38.44%	12.47% / 5.55% / 13.59% / 10.85% / 9.67%	12.10% / 5.72% / 13.24% / 9.86% / 9.61%	4.44% / 2.32% / 3.02% / 2.64% / 2.46%
87.02% / 89.20% / 92.97% / 94.13% / 94.93%	71.85% / 65.98% / 54.50% / 42.49%	9.61% / 5.83% / 13.40% / 11.32% / 14.89%	8.81% / 5.66% / 12.90% / 11.04% / 14.07%	3.77% / 1.85% / 2.66% / 2.06% / 2.73%
86.68% / 89.91% / 93.81% / 94.40% / 95.52%	74.17% / 68.06% / 55.25% / 42.87%	10.36% / 8.47% / 17.39% / 13.83% / 16.14%	9.96% / 8.26% / 16.67% / 13.37% / 14.75%	3.53% / 1.98% / 2.65% / 1.96% / 2.78%
89.62% / 90.31% / 92.51% / 93.57% / 92.68%	75.08% / 71.16% / 61.31% / 47.72%	4.62% / 3.12% / 3.45% / 3.08% / 5.83%	4.78% / 3.22% / 3.31% / 3.11% / 5.54%	2.69% / 1.84% / 1.95% / 1.72% / 1.95%
90.27% / 90.37% / 91.69% / 92.74% / 92.85%	71.17% / 66.82% / 58.91% / 47.71%	5.25% / 3.70% / 3.26% / 3.52% / 4.47%	5.47% / 3.65% / 3.00% / 3.45% / 4.09%	2.73% / 1.81% / 1.87% / 1.76% / 1.62%
84.31% / 87.58% / 88.01% / 89.42% / 92.29%	75.19% / 69.42% / 58.89% / 46.21%	8.62% / 12.59% / 11.38% / 10.84% / 17.52%	8.53% / 11.84% / 10.12% / 10.67% / 15.58%	2.43% / 2.13% / 3.26% / 2.31% / 1.77%
90.40% / 86.80% / 92.70% / 94.70% / 95.36%	74.94% / 69.07% / 57.80% / 44.71%	9.08% / 1.49% / 6.77% / 11.95% / 19.70%	8.90% / 1.48% / 6.84% / 11.60% / 17.43%	3.26% / 0.91% / 2.70% / 2.24% / 1.91%
89.98% / 90.84% / 94.80% / 95.98% / 97.27%	83.57% / 78.62% / 70.64% / 60.37%	9.43% / 9.62% / 18.17% / 13.77% / 25.71%	9.03% / 8.95% / 17.29% / 13.92% / 24.87%	3.18% / 2.35% / 3.44% / 2.54% / 2.26%
95.34% / 94.80% / 96.75% / 95.59% / 95.54%	82.50% / 74.92% / 62.05% / 47.49%	12.60% / 9.80% / 10.15% / 11.00% / 14.00%	11.77% / 9.27% / 10.01% / 10.12% / 12.66%	3.97% / 1.68% / 1.78% / 1.73% / 1.43%

Simultaneous Multiple-Row Activation

Recent works experimentally demonstrate a new phenomenon called **SiMRA to realize operations** in-DRAM

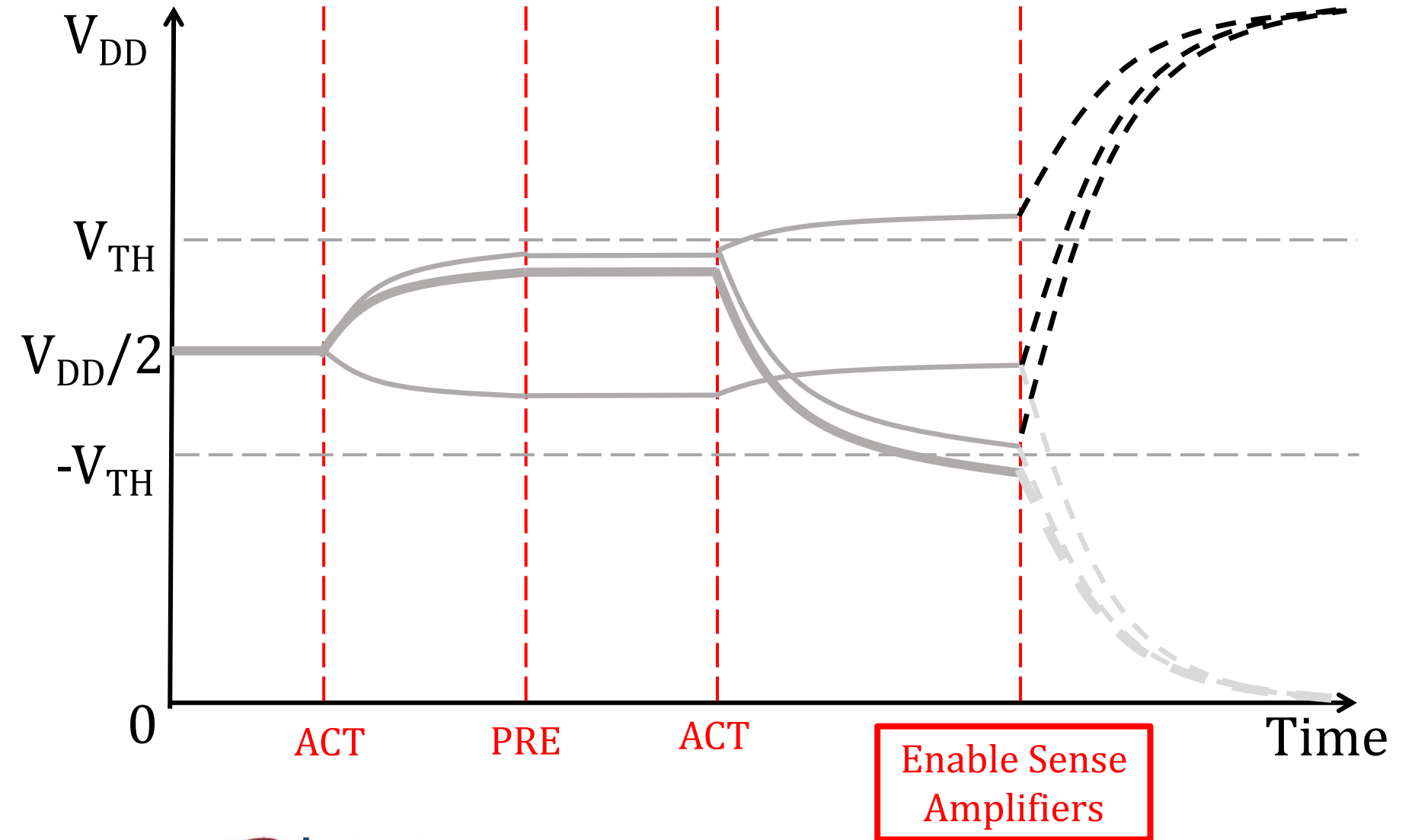
- Carefully engineered sequence of DRAM commands allows DRAM to exhibit out-of-spec behavior
- Prior work shows that SiMRA can be used to perform **many operations**
 - Data copy & initialization
 - Bulk bitwise operations
 - True random number generation
 - ...

Generating Signatures via SiMRA



Enable Sense Amplifiers

Generating Signatures via SiMRA



Limitations of Tested COTS DRAM Chips

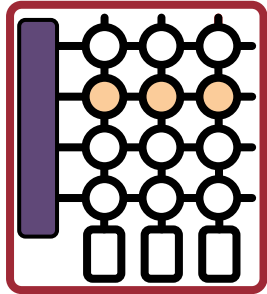
- **Some COTS DRAM chips do not support all in-DRAM operations**
 - We do not observe simultaneous multiple-row activation in 32 tested Samsung & Micron chips
- Hypothesis
 - Internal DRAM circuitry ignores the PRE command or the second ACT command when the timing parameters are greatly violated

**If such a limitation were not imposed,
we believe these DRAM chips would also be
fundamentally capable of performing the operations
we examine in this work**

Hypothesis: Row Decoder Circuitry

Simultaneous many-row activation is possible due to the **hierarchical DRAM row decoder design**

DRAM Subarray



Row Address



Row Decoder

Wordline



Row Address (RA)



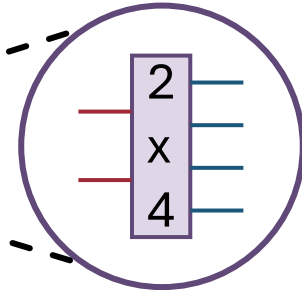
Stage 1 Decoder

Stage 2 Decoder

Stage 3 Decoder

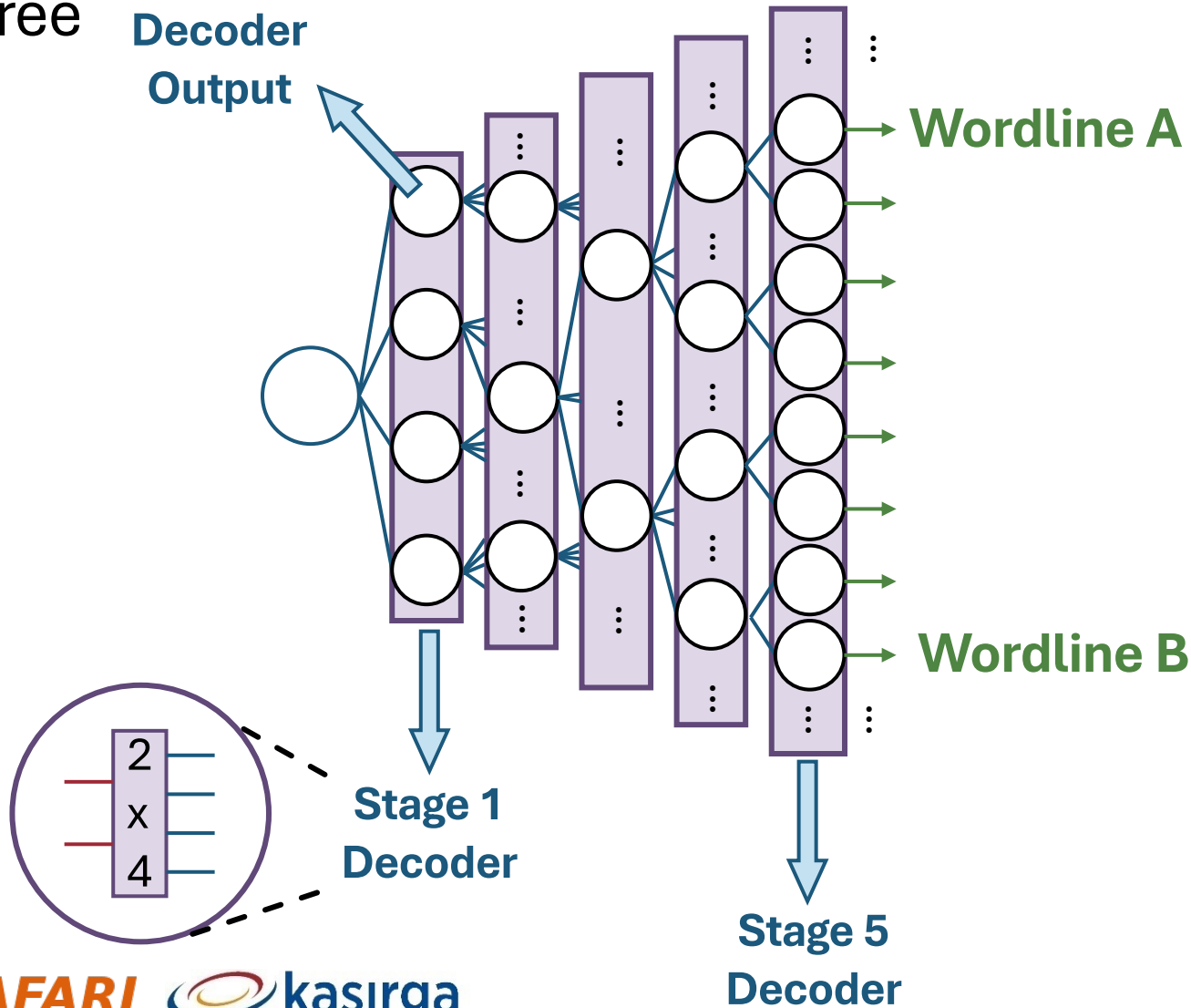
Stage 4 Decoder

Stage 5 Decoder

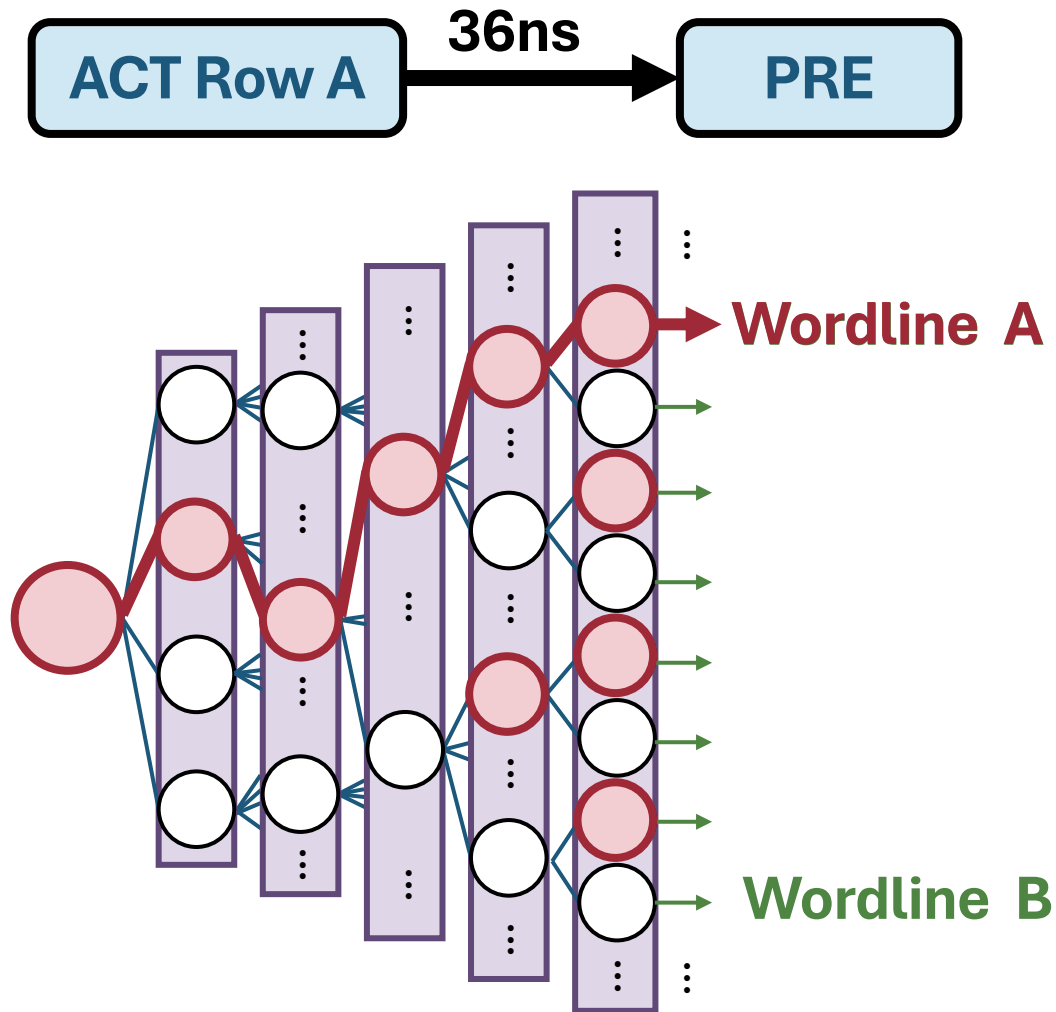


Row Decoder: A Tree Example

- We can visualize the hierarchical row decoder circuitry as a tree



Activating a Single Row



1. Decode
Row A address

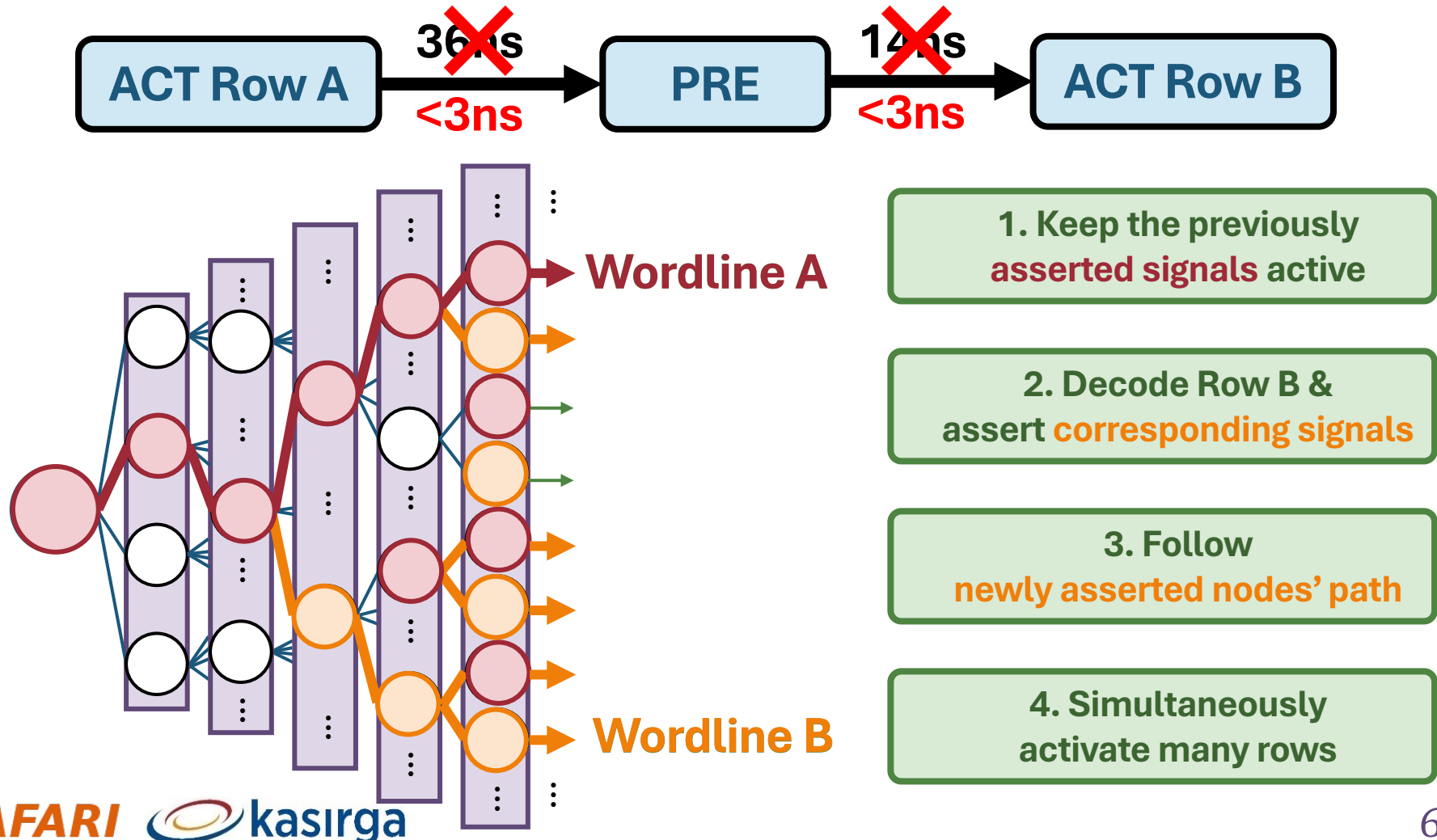
2. Assert
corresponding signals

3. Follow
asserted nodes path
from root to leaf

4. Assert wordline

Activating Many Rows: A Walkthrough

Back-to-back ACT commands with violated timings
asserts many more signals in the row decoder



Simultaneous Multiple-Row Activation

